SGT3012-2

ANGLE ENCODER UNIT (516126-02) LOWEST REPLACEABLE UNITS (NSGT)

DEPOT MAINTENANCE HANDBOOK

SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6
SIGNAL CONDITIONING BOARD P/N 206497-13
SIN/COS NETWORK BOARD P/N 206499-1
SUCCESSIVE APPROXIMATION BOARD P/N 206498-1
ADDRESS COMBINATION BOARD P/N 209508-1
DUAL OUTPUT REGISTERS BOARD P/N 212194-2
ADDER/COMPLEMENTER BOARD P/N 212814-1
10^2 TO 10^{-2} BINARY/BCD BOARD P/N 207730-2
10^{-3} BINARY/BCD BOARD P/N 207733-3
DIFFERENTIAL LINE DRIVER BOARD P/N 212815-1
1200 HZ OSCILLATOR BOARD P/N 211190-5
±15 VDC POWER SUPPLY ASSEMBLY R115
+5 VDC POWER SUPPLY ASSEMBLY 210
EXTENDER BOARD ASSEMBLIES P/N 212189-1 AND P/N 211300-1

CONTRACT NO.
CB-1978-5052-S3G

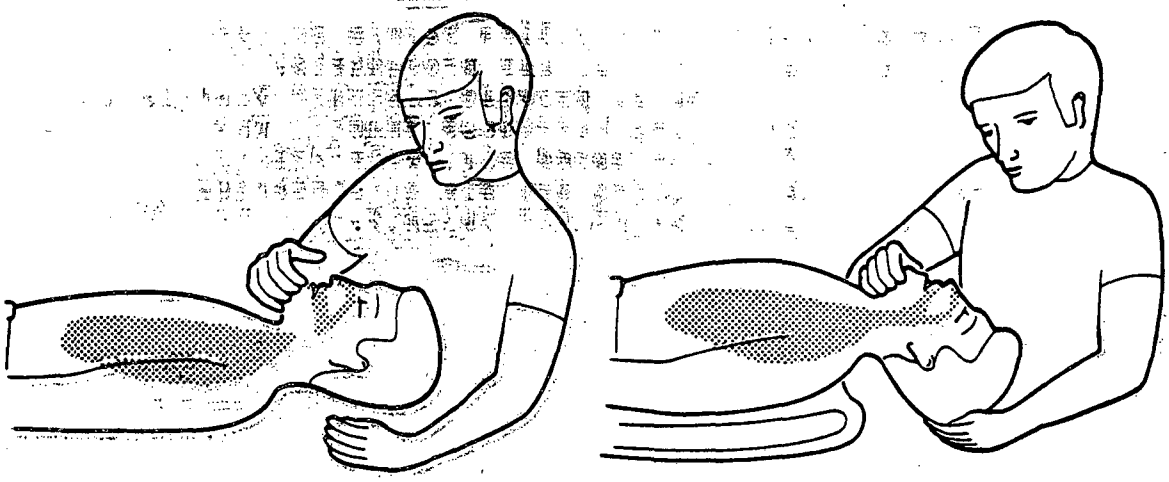
1 MARCH 1983

TREATMENT FOR ELECTRICAL SHOCK

WHEN BREATHING HAS STOPPED

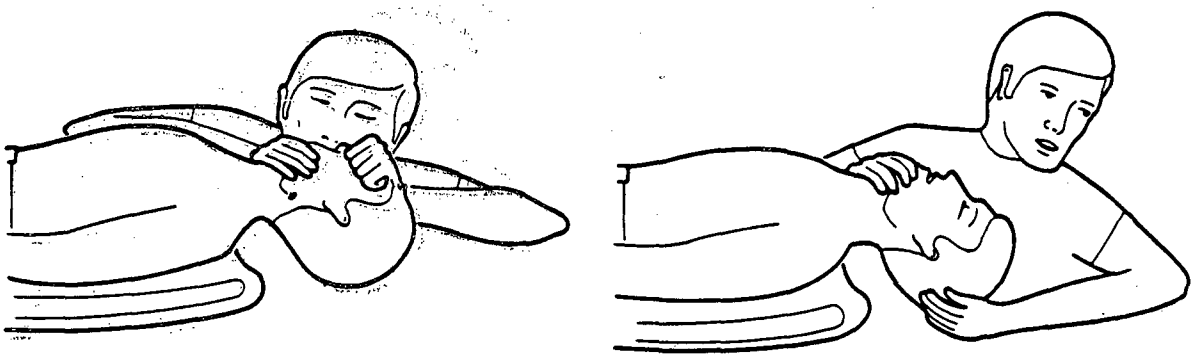
1. INITIAL PROCEDURE

Switch off the current. If this is impossible free the person using something made of rubber, cloth or wood or a folded newspaper; use the casualty's own clothing if dry. Do not touch his skin before the current is switched off. If the victim's breathing has stopped IMMEDIATE EFFORT to restart it is essential. EVERY SECOND COUNTS.



2. STARTING POSITION

Victim face up. Tilt head back and pull chin forward to open air passages.



3. INFLATION

Seal victim's nose by pinching nostrils. Open your mouth wide and inflate the victim's lungs by blowing air into his mouth.

4. EXHALATION

When you see the victim's chest rise remove your mouth to allow the air to escape from his lungs, and turn your head to one side. Continue with 3 & 4 until natural respiration returns.

Do not exceed 10-12 breaths per minute. If stomach contents are regurgitated, turn the victim's head to one side and clean out his mouth. When there are signs of natural respiration returning adjust your breathing to coincide with the victim.

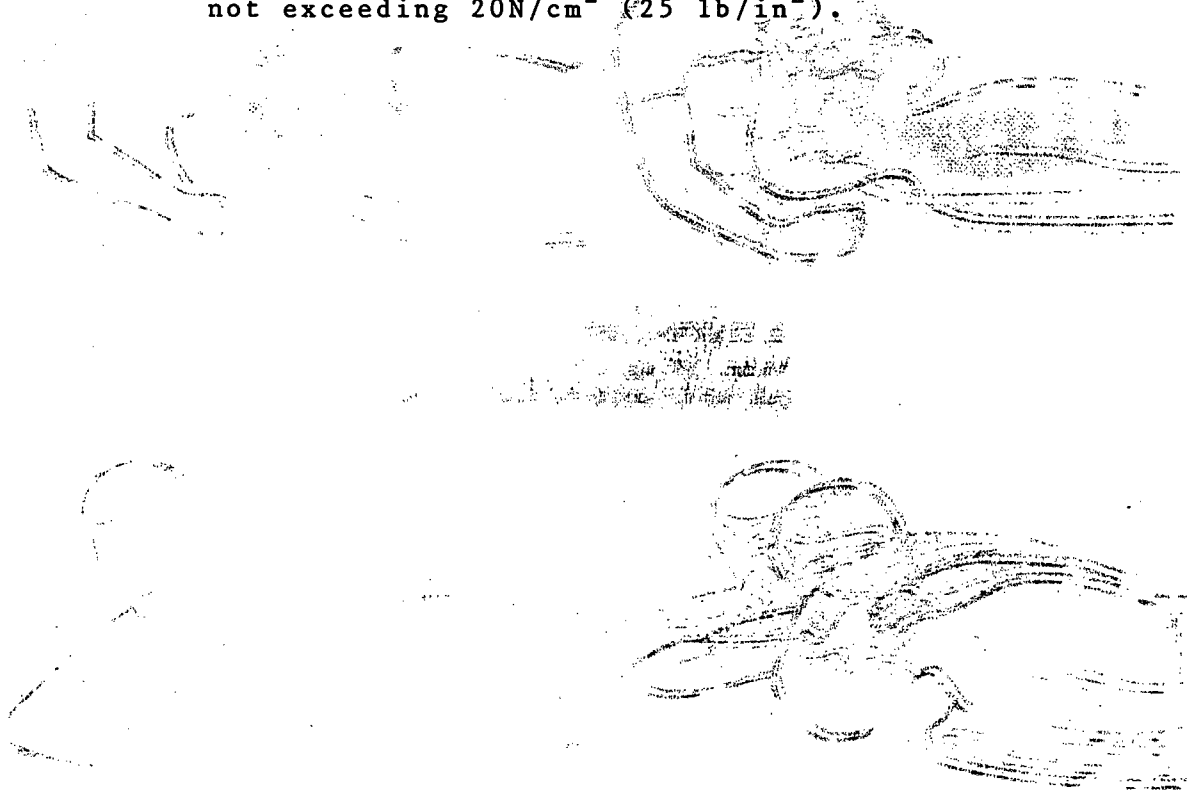
SAFETY WARNING PAGE

WARNING

Hazardous ac line voltage is present at the power input. Use extreme caution when making adjustments and measurements.

WARNING

Turn off all power supplies before carrying out any cleaning or repair procedures. When using solvents, provide adequate ventilation and avoid breathing hazardous fumes. When cleaning with compressed air, wear safety goggles and use clean dry air at a pressure not exceeding 20N/cm^2 (25 lb/in^2).



AMENDMENT HISTORY PAGE

Insert latest amendment pages; dispose of superseded pages in accordance with applicable regulations.

NOTE

On an amendment page, the portion of the text affected by the latest change is indicated by a vertical line, or other change symbol, in the outer margin of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Total number of pages in this handbook is 213, consisting of the following

Page No.	Amendment No.	Page No.	Amendment No.
i-xx	0		
1-i - 1-vii	0		
1-viii blank	0		
1-1 - 1-104	0		
2-i - 2-vi	0		
2-1 - 2-41	0		
2-42 blank	0		
2-43 - 2-61	0		
3-i	0		
3-ii blank	0		
3-1 - 3-12	0		

Zero in this column indicates an original page.

RECORD OF MODIFICATION

ECO	TITLE	AMENDMENT TO HANDBOOK

INTRODUCTION

This handbook contains instructions for the offsite maintenance of the Antenna Subsystem Angle Encoder Unit LRU. References are contained within this handbook to the General Offsite Maintenance Handbook SGT 3003-3. The handbook is divided into three parts.

Part 1 contains technical details and is divided into two sections. Section I contains the circuit analysis and Section II contains the mechanical description.

Part 2 contains the maintenance and repair procedures and is divided into seven sections. Section I contains performance test/fault isolation instructions; Section II contains disassembly and reassembly instructions; Section III contains repair procedures; Section IV contains alignment and adjustment instructions; Section V contains calibration procedures; Section VI contains postrepair checkout instructions and Section VII contains packaging/packing instructions for reshipment of an LRU.

Part 3 contains lists of the electrical, electronic and mechanical components of the LRU's segregated into the different modules in which they are fitted.

GLOSSARY OF ABBREVIATIONS

	A
ac	Alternating Current
	B
BCD	Binary Coded Decimal
	C
CLK	Clock
COM	Common
	D
DAC	Digital to Analogue Converter
dc	Direct Current
	E
EC	'End Conversion'
EOC	End of Conversion
	F
FET	Field Effect Transistor
	G
	H
Hz	Cycle
	I
IC	Integrated Circuit
in	Inch
I/P	Input
	K
K	Kelvin
k	Kilo (1000)
	L
lb	Pound (weight)
lb/in^2	Pounds per Square Inch
LED	Light Emitting Diode
LRU	Lowest Repairable Unit
LSB	Least Significant Bit

GLOSSARY OF ABBREVIATIONS (continued)

	M
MSB	Most Significant Bit
	N
N/A	Not Applicable
	O
O/P	Output
	P
p-p	Peak-to-Peak
Pres	Pressure
PSU	Power Supply Unit
	Q
QTY	Quantity
	R
Ref	Reference
Reg	Regulator
	S
Sec	Second
SC	Start Conversion
sig	Signal
	T
TBS	To Be Supplied
TTL	Transistor Transistor Logic
	U
uS	Microsecond
	V
Vac	Volts Alternating Current
Vdc	Volts Direct Current

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PART 1

TECHNICAL DESCRIPTION

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PART 1

SECTION I

CIRCUIT ANALYSIS

1.1 GENERAL

This section contains a detailed circuit analysis for each LRU assembly of the angle encoder unit which can be repaired using depot facilities. Also included is a table of integrated circuits (IC's) used within each LRU.

1.2 REPAIR LEVELS

This paragraph defines the depot repairable, throwaway and factory repairable items of the angle encoder unit.

1.2.1 DEPOT REPAIRABLE

a. Synchronous Demodulator/Multiplexer Board P/N 212195-6.

b. Signal Conditioning Board P/N 206497-13

c. Sin/Cos Network Board P/N 206499-1

d. Successive Approximation Board P/N 206498-1

e. Address Combination Board P/N 209508-1

f. Dual Output Registers Board P/N 212194-2

g. Adder/Complementer Board P/N 212814-1

h. 10^{2} to 10^{-2} Binary/BCD Board P/N 207730-2

i. 10^{-3} Binary/BCD Board P/N 207733-3

j. Differential Line Driver Board P/N 212815-1

k. 1200 Hz Oscillator Board P/N 211190-5.

l. $\pm$15 Vdc Power Supply Assembly R115 (PS1).

m. +5 Vdc Power Supply Assembly 210 (PS2).

n. Extender Board Assemblies P/N 212189-1 and P/N 211300-1

1.2.2 FACTORY REPAIRABLE

None

1.2.3 THROWAWAY ITEMS

Chassis/pcb mounted components can be disposed of locally.

1.3 CIRCUIT ANALYSIS

Analogue data representing antenna azimuth and elevation is received by the angle encoder unit as sine and cosine (coarse and fine) 1200 Hz inputs. These inputs are demodulated to produce dc levels which are time-division multiplexed into separate sine and cosine outputs representing azimuth fine, azimuth coarse, elevation fine and elevation coarse data. The multiplexed data is converted into 13-bit digital format; coarse data has a value of 180^{o} (MSB) to 0.043^{o} (LSB), fine data has a value of 5.625^{o} (MSB) to 0.001^{o} (LSB).

Certain circuit boards of the angle encoder process azimuth data only or elevation data only. Other boards process fine and coarse azimuth and elevation data at different times in the conversion sequence. Throughout the remainder of this description, angles and sequences refer to coarse data unless otherwise stated.

The following paragraphs contain detailed circuit analysis for each LRU and are referenced to schematic diagrams included at the end of part 1.

1.3.1 SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6

This board demodulates angle data inputs (coarse sine and cosine, fine sine and cosine) to produce dc outputs with amplitudes and polarities proportional to the angle data inputs. These dc outputs are combined to provide time-division multiplexed cosine and sine outputs.

1.3.1.1 Circuit Description. A simplified block diagram of the board is shown in figure 1-1. The four synchronous demodulators are similar and the two output switching circuits (coarse and fine) are identical. All four demodulators are supplied with a common (synchronizing) 1.2 kHz waveform. This circuit description details the signal path for a coarse-sine input. The coarse SIN input to board pins CC and BB is a 1.2 kHz sinewave, amplitude-modulated by the coarse-sine angle data (see figure 1-2). This input is passed to differential amplifier U2, which provides a gain of 2 (1.3 for the 'fine' demodulator circuits) and rejects unwanted common-mode signals. From U2-6 the signal is passed to PNP transistor switch Q1, and through an inverting, unity-gain stage U1 to NPN switch Q2. Q1 and Q2 are switched on and off alternately by a $\pm$ 13 V 1.2 kHz reference output from Q10 emitter. The resultant output at Q1/Q2 emitters is a full-wave rectified dc voltage. This output is smoothed by low-pass filter R62, C2 and passed through non-inverting, unity-gain buffer stage U10 to analogue switch U11.

PART 1

SECTION I

CIRCUIT ANALYSIS

1.1 GENERAL

This section contains a detailed circuit analysis for each LRU assembly of the angle encoder unit which can be repaired using depot facilities. Also included is a table of integrated circuits (IC's) used within each LRU.

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This paragraph defines the depot repairable, throwaway and factory repairable items of the angle encoder unit.

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i. 10^{-3} Binary/BCD Board P/N 207733-3

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l. $\pm$15 Vdc Power Supply Assembly R115 (PS1).

m. +5 Vdc Power Supply Assembly 210 (PS2).

n. Extender Board Assemblies P/N 212189-1 and P/N 211300-1

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None

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Chassis/pcb mounted components can be disposed of locally.

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Analogue data representing antenna azimuth and elevation is received by the angle encoder unit as sine and cosine (coarse and fine) 1200 Hz inputs. These inputs are demodulated to produce dc levels which are time-division multiplexed into separate sine and cosine outputs representing azimuth fine, azimuth coarse, elevation fine and elevation coarse data. The multiplexed data is converted into 13-bit digital format; coarse data has a value of 180° (MSB) to 0.043° (LSB), fine data has a value of 5.625° (MSB) to 0.001° (LSB).

Certain circuit boards of the angle encoder process azimuth data only or elevation data only. Other boards process fine and coarse azimuth and elevation data at different times in the conversion sequence. Throughout the remainder of this description, angles and sequences refer to coarse data unless otherwise stated.

The following paragraphs contain detailed circuit analysis for each LRU and are referenced to schematic diagrams included at the end of part 1.

1.3.1 SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6

This board demodulates angle data inputs (coarse sine and cosine, fine sine and cosine) to produce dc outputs with amplitudes and polarities proportional to the angle data inputs. These dc outputs are combined to provide time-division multiplexed cosine and sine outputs.

1.3.1.1 Circuit Description. A simplified block diagram of the board is shown in figure 1-1. The four synchronous demodulators are similar and the two output switching circuits (coarse and fine) are identical. All four demodulators are supplied with a common (synchronizing) 1.2 kHz waveform. This circuit description details the signal path for a coarse-sine input. The coarse SIN input to board pins CC and BB is a 1.2 kHz sinewave, amplitude-modulated by the coarse-sine angle data (see figure 1-2). This input is passed to differential amplifier U2, which provides a gain of 2 (1.3 for the 'fine' demodulator circuits) and rejects unwanted common-mode signals. From U2-6 the signal is passed to PNP transistor switch Q1, and through an inverting, unity-gain stage U1 to NPN switch Q2. Q1 and Q2 are switched on and off alternately by a $\pm$ 13 V 1.2 kHz reference output from Q10 emitter. The resultant output at Q1/Q2 emitters is a full-wave rectified dc voltage. This output is smoothed by low-pass filter R62, C2 and passed through non-inverting, unity-gain buffer stage U10 to analogue switch U11.

The output from U11-5 is combined with the output from U14-5 (coarse and fine data) to produce a time-multiplexed MPLX SIN output at board pin 8. The switches are operated when the appropriate select coarse or fine input is at '1'. These inputs are of 500us duration, and occur at the intervals shown in the timing diagram, figure 1-3.

A 1.2 kHz, 10.4 V p-p reference waveform input at board pin F is clipped by CR2 and CR1, amplified by U9 and passed to push-pull current driver stage Q9, Q10. The output produced at Q9/Q10 emitters is a 1.2 kHz ± 13 V square waveform. This waveform provides the reference input to all four synchronous demodulator circuits, and a REF. SQ. OUT output at board pin R.

1.3.2 SIGNAL CONDITIONING BOARD P/N 206497-13

This board produces TTL compatible outputs representing the polarities of sine and cosine input signals. The sine and cosine inputs are processed to produce negative sine/positive cosine outputs regardless of input polarity. A 660 kHz clock signal for external circuit use is also generated by this board. Phase relationships of the input and output signals are shown in figure 1-5.

1.3.2.1 Circuit Description. Sine and cosine signal processing circuits are similar, the only difference being the polarity of output. Only one multiplexed input (sine) is described in detail. The multiplexed sine MPLX SIN input signal at board pin X is passed to high-impedance, unity-gain buffer stage A3 (see figure 1-4). Potentiometer R15 is used to adjust A3 offset (0V output at test point board pin J, with board pin X grounded). The buffered output is passed to:

Sine polarity stage A4.

Sine continuous stage A2.

In A4, the sine signal is compared with a dc level (0V nominal), applied to A4 non-inverting input from divider R31 and R32. If the signal at board pin X is greater than 0V (0° to 180°), A4 output goes low cutting off output switch Q13, and a +4 V SIN POL output is produced at board pin 5. Alternatively, if the input at board pin X goes below 0V (180° to 360°), Q13 conducts and the output at board pin 5 goes to 0V. The output at board pin 5 therefore represents the sine signal polarity. The cosine signal MPLX COS is processed in a similar circuit and produces a cosine polarity COS POL output at board pin D. The two polarity signals are processed externally and returned to board pins H (SIN CONT) and E (COS CONT) with the following phase relationships (figure 1-5).

Polarity Sin	Cos	Quadrant
-	+	0° - 90°
-	-	90° - 180°
+	-	180°C - 270°C
+	+	270°C - 360°C

The SIN CONT signal is passed to a level converter stage formed by Q12 and Q11. This stage produces switching outputs at suitable levels (-15 V, +5 V) to operate FET switches Q9 and Q8. With a low input at board pin H (0° to 180°) Q12 conducts, switching on Q9, and Q11 cuts off, switching off Q8. The output from A3 is then passed via Q9 and R13 to A2-3. A2 therefore inverts the input from A3 and a negative (SIN) dc waveform is produced at Q10 emitter. Alternatively, a high input at board pin H (180° to 360°) causes Q9 to cut off and Q8 to switch on. The negative output from A3 is then passed without inversion through A2, and again produces a negative waveform from Q10 emitter. The output at Q10 emitter is, therefore, always a negative dc output, irrespective of the polarity of the input at board pin X. The cosine input COS CONT processed in an identical circuit except that the output stage, Q16, is a PNP type transistor. The output at Q16 emitter (COS) is therefore always a positive dc level.

A 660 kHz oscillator circuit is formed by R10, C3, Q6 and controlled by transistor switch Q5. Q5 is cut off when the end of conversion (EC) input at board pin 21 goes low. C3 then charges towards +15 V with a time constant determined by R10. When the charge on C3 is sufficient to trigger Q6, C3 discharges to ground through Q6. The resultant output from Q6 is a square wave at a frequency of 660 kHz. Output switch Q7 provides a TTL compatible (+5 V, 0V) clock output at board pin 10. When the EC input goes high, Q5 conducts, C3 then discharges through Q5 to 0V, inhibiting the clock signal output.

1.3.3 SIN COS NETWORK BOARD P/N 206499-1

This board samples analogue (sine and cosine) angular data inputs during the selected conversion sequence to produce angular output data in 11-bit serial binary format at TTL levels. The relative amplitudes and phase relationships of the cosine (COS) and sine (SIN) signals applied to the cosine and sine ladder networks are shown in figure 1-5.

1.3.3.1 Circuit Description. The cosine ladder consists of an analogue-to-digital converter formed by twelve NPN transistor stages (Q12 to Q24) (see figure 1-6). The transistors are controlled by logic '1' or logic '0' gating signals, applied

through NPN switch drivers (Q25 to Q36) from the $2^{1}X$ to $2^{11}X$ (inverted) and $2^{\overline{12}}$ control inputs to the board. The collectors of Q12 to Q24 are connected in parallel to the cosine signal (COS) input at board pin 11, and the emitter loads are connected to a summing point at R36. Each stage only conducts when the instantaneous amplitude of the cosine input is sufficiently high to enable the stage to be forward-biassed by the control input. The values of the emitter load resistors are selected such that, if more than one stage is conducting, the potential at the summing point remains constant.

The sine ladder is similar to the cosine ladder, except that PNP transistors are used instead of NPN types. The ladder receives the same control inputs as the cosine ladder, and emitter loads are connected to a common summing point at R85.

Because the same control signal is applied to both ladders, one transistor stage conducts and the corresponding stage in the other ladder cuts off. The output of R36, R85 junction is therefore positive (cosine ladder active) or negative (sine ladder active) with reference to signal ground. This output is limited by CR1 and CR2 and then compared in A1 with a dc reference level, applied from offset control R31. The comparator output at A1-6 is passed via level converter output stage Q11, to provide a TTL compatible (+5 V, 0V) output at board pin 20.

At the start of the conversion sequence, the first control input applied is a $2^{11}X$ signal at board pin 17 representing an angle of 45^{o}. Assuming that this input is at logic '0' and the instantaneous cosine input is sufficiently high (greater than an angle of 45^{o}), Q12/Q13 conducts. A1-6 goes to logic '0' and a logic '1' is passed from Q11 collector to an external register. The external register stores the logic '1', maintains the $2^{11}X$ control input at logic '0' and sends a logic '0' $2^{10}X$ (22.5^{o}) control input to board pin 16.

If the cosine signal is less than 45^{o}, a logic '0' is passed to the external register. The external register then stores the logic '0', changes the $2^{11}X$ control input to logic '1' and sends a logic '1' $2^{10}X$ control signal to board pin 16.

Control input $2^{10}X$ is followed in sequence by control inputs $2^{9}X$ (11.25^{o}) to $2^{1}X$ (0.043^{o}). As each control input samples the input signal, the logic '1'/'0' outputs produced from Q11 are stored in the external register, and the appropriate logic '1'/'0' control signals are generated for the next LSB conversion. After control input $2^{1}X$ has been processed, the conversion sequence is complete, with the 11-bit binary word, equivalent to the angle input, stored in the external register. Offset control R31 is adjusted so that with a 45^{o} input the output at A1-6 just switches to give a logic '0' output.

1.3.4 SUCCESSIVE APPROXIMATION BOARD P/N 206498-1

This board provides sequential control outputs that are used in an external digital-to-analogue converter (successive approximation circuit) to sample fine and coarse azimuth and elevation angle data. The binary output produced by the converter is stored and the binary equivalent of the sampled data angle is output in 13-bit parallel format.

1.3.4.1 Circuit Description. A conversion sequence is initiated by the start conversion (SC) signal of 10us duration applied at board pin 7 (see figures 1-7 and 1-21). At this time, the end-of-conversion (EC) input at board pin 9 is at logic '0' and a logic '1' is produced from U10-4 and a logic '0' from U4-6. The SC signal therefore produces a logic '1' output from U16-6 to set JK bistable U6-15 to logic '1'. This signal is applied to U2-9 (SC) and U5-10 (MR) to initiate the conversion sequence. The SC signal also sets U6-1 to logic '1', provided that an initial switch-on delay period (determined by C3 and R5) has expired.

After 10us, the SC signal returns to logic '0', removing the set inputs to the two JK bistables. The unilock input at board pin 10 is then divided by two to give a train of clock pulse outputs from U6-1. This output is applied as the clock inputs to U2-7 and U6-13 and passed to board pin 8. The input to U6-13 clears U6 and resets the signal at U6-15 to logic '0'.

When the end of conversion (EC) input at board pin 9 becomes logic '1', a logic '0' is produced at U10-4 coincident with the logic '0' to logic '1' transition of the clock input at U10-6, and a logic '1' from U4-6 is passed to U16-4. The SC input at U16-5 is now at logic '0', and the logic '1' produced at U16-6 again sets U6-5 to logic '1', terminating the conversion sequence.

U2 and U5 are 8-bit registers, with U2 restricted to 6-bit operation by a connection between U2-10 (FF) and U2-13. The two modules are connected in series to operate as the successive approximation register. Stages Q6, Q4 and Q3 of U2 are not used externally and the register produces an 11-bit output, although 14 clock pulses are required to shift the data through all stages.

A conversion sequence is initiated by a logic '1' applied to U2-9 (SC) and U5-10 (MR) from U6-15. Data from U1-6 is then entered into U2 on the positive transition of the clock input from U6-1, and the Q outputs of U5 are reset to logic '0's. Conversion continues after the logic '1' input at U2-9 returns to logic '0' until, after six clock periods, U2-11

goes to logic '1' and data stored in U2 is retained. This logic '1' is applied to U5-9 enabling data to be clocked into U5. When 8 bits have been transferred, U5-11 goes to logic '1' signalling the end of the conversion sequence, and data stored in U5 is retained. The logic '1' output from U5-11 is passed through inverters to produce the end of conversion (EC) output at board pin E. Board pin E is externally linked to board pin 9, and the EC signal terminates the conversion sequence.

The data outputs from the register are applied through inverting buffers and exclusive OR gates to provide control outputs from the board. Control outputs $2^{11}X$ to $2^{1}X$ and A to E provide sampling outputs to the external digital-to-analogue converter. The outputs produced from the converter in response to the sampling inputs are fed back in serial form as the data (COMP OUT) input at board pin Z. This input is passed through an exclusive OR gate formed by U12 (pins 1, 2, 3) and inverter U1 (pins 6, 7) to the data input of U2. The first data input represents the $2^{11}X$ (45^{o}) sample. This bit is stored and the value (logic '1' or '0') determines the value of the next ($2^{10}X$) control output. The process is continued for all bits until, after the $2^{1}X$ sample is received, the register contains the binary equivalent of the sampled angle data. These outputs are passed through inverters to provide the 11 least significant bits (2^{11} to 2^{1}) of the 13-bit output from the board. The other two bits are produced by the quadrant detector circuit.

U11, exclusive OR gate U16 (pins 11, 12, 13) and associated inverters form a quadrant detector circuit, which determines the value of the two most significant bits (2^{13} and 2^{12}) of the 13-bit output.

When U11 is clocked by a logic '1' output derived by inverters U15 and U1 from U2-2, the sine polarity (SIN POL) and cosine polarity (COS POL) inputs at board pins 2 and 3 appear at U11-9 (sine), U11-5 (cosine) and U11-8 (inverted sine). U11-8 output provides the continuous sine (SIN CONT) output at board pin B, and is inverted to produce an output at board pin D. This output forms bit 2^{13} of the 13-bit output, where logic '1' represents angle data within 0^{o} to 180^{o}, and logic '0' represents data within 180^{o} to 360^{o}.

U11-5 output provides a continuous cosine (COS CONT) output at board pin C, and is passed with U11-9 output to an exclusive OR gate U16 (pins 11, 12, 13). U16 produces a logic '1' output when both inputs are different to each other. This output is passed through inverters to form bit 2^{12} of the 13-bit output word, where logic '1' represents angle data within 90^{o} to 180^{o} or 180^{o} to 270^{o}, and logic '0' represents data within 0^{o} to 90^{o} and 270^{o} to 360^{o}. An inverted ($\overline{2^{12}}$) output is also produced at board pin J.

1.3.5 ADDRESS COMBINATION BOARD P/N 209508-1

This board performs the following functions:

a. Generates 'start of conversion' pulses with duration of 10usec, spaced at intervals of 2ms (nominal). During each 2 millisecond conversion period, generates select fine azimuth, select coarse azimuth, select fine elevation and select coarse elevation segmentV signals at intervals of 500usec. These signals are used by external multipliers to select the data for conversion at the appropriate time between SC pulses.

b. Receives 'end of conversion' (EC) pulses, with duration of 30usec spaced at 500usec intervals between successive SC pulses.

c. Stores 'fine' angle data, applied to the board in 13-bit parallel-binary format during the appropriate 500usec conversion sequence.

d. Combines the stored fine data with 'coarse' angle data, applied to the board in 13-bit binary format during the next 500usec conversion, sequence to produce an 18-bit output representing angles between 0^{o} and 360^{o} with a resolution of 0.001^{o}.

e. Generates data ready and register update signals with a duration of 10usec at the end of azimuth and elevation conversion sequences, ie at 1msec intervals.

f. Ambiguity logic is included to ensure that resolution errors are not introduced when combining the coarse and fine data inputs.

1.3.5.1 Circuit Description. Oscillator module U7 generates a waveform at 2msec intervals, that determines the start and finish of a data conversion period (see figure 1-8). The output of U7-3 is inverted by U6 and passed from board pin U as the SC signal (refer to figure 1-3). The output of U7-3 also clears ripple counter U4 at the start and finish of the data conversion period.

An end of conversion (EC) input is applied at board pin 10 at four 500us intervals during the conversion period. This input is passed through inverter stages to provide an inverted clock input to U4-6, an inverted output ($\overline{EC}$) at board pin F and an inverted clock input to a 13-bit register formed by U18, U17, U16 and U13.

In U4, each clock input advances the binary count output at U4-9, U4-2 and U4-12. These outputs are decoded in U3 and passed through inverters to provide logic '1' outputs from the board as follows:

Binary Count	Output	Board Pin
000	Select fine (Azimuth)	20
001	Select coarse (Azimuth)	21
010	Select fine (Elevation)	cc
011	Select coarse (Elevation)	12
100	Stop clock	Y

During the azimuth fine and elevation fine segments of the period, a logic '1' output is produced from NAND gate U2 (pins 13, 12, 11). This logic '1' is applied to the load input of the 13 bit register, and enables the fine azimuth or fine elevation data inputs (bits 2^1 - 12^{13}) to be loaded into the 13-bit register on the logic '1' to '0' transition of $\overline{EC}$.

During the azimuth coarse and elevation coarse segments of the period, a logic '1' output is produced from NAND gate U2 (pins 4, 5, 6). At the end of each coarse segment, the logic '1' to logic '0' transition at U2-6 causes a logic '1' pulse of 10usec duration to be produced from monostable U8-6. This pulse is gated with the logic '1' SELECT FINE (ELEVATION) and logic '1' STOP CLOCK outputs to produce logic '0' AZ REG UPDATE and EL REG UPDATE outputs from board pins 22 and Z. These outputs are also inverted to produce logic '0' AZ DATA READY and EL DATA READY signal outputs at board pins AA and 25.

The three MSB's of stored fine data (bits 2^{13}, 2^{12}, and 2^{11}) are decoded in U9, and the decoder outputs are passed to a gating circuit. During a coarse data segment the five MSB's of coarse data input (bits 2^{13} to 2^9) are passed to a 5-bit adder formed by U14 and U15. Coarse data bits 2^8, 2^7 and 2^6 are decoded in U12, and the decoder outputs are passed to the gating circuit.

The gating circuit is formed by six NAND gates in U10 and U11, and two inverters in U5. The circuit compares the outputs from the decoders, and produces suitable control outputs to modify the output from the 5-bit adder (U14, U15). U5-6 provides the 'carry' input to the adder (U15-13), and U5-8 output is added in the adder to each bit of the 5 MSB's of the coarse data input. Operation of the gating circuit and adder is shown in the following examples.

a. Assume that the value of the three MSB's of stored fine data is 010. In this condition, U10-12 is at logic '1' and U10-6 is at logic '0'.

b. If the value of bits 2^8 to 2^6 of coarse data is 000 (less than fine data):

U11-12 = '1' U11-8 = '0'
U11-6 = '0' U10-9 = '1'
U5-8 = '1' U5-6 = '0'

The adder then subtracts one bit (LSB) from the coarse data input, as follows:

	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}
Coarse data input	1	1	1	0	1	0	0	0
Carry input from U5-6					0			
Summing input from U5-8	1	1	1	1	1			
Adder Output	1	1	1	1	0	0		

c. If the value of bits 2^8 to 2^6 of coarse data is 010 (equal to fine data):

U11-12 = '1' U11-8 = '0'
U11-6 = '1' U10-8 = '1'
U5-8 = '0' U5-6 = '0'

The coarse data input is therefore unchanged by the gating inputs as follows:

	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}
Coarse data input	1	1	1	0	1	0	1	0
Carry input from U5-6					0			
Summing input from U5-8	0	0	0	0	0			
Adder Output		1	1	1	0	1		

d. If the value of bits 2^8 to 2^6 of coarse data is 111 (greater than fine data):

U11-12 = '0' U11-8 = '1'
U11-6 = '1' U10-8 = '0'
U5-8 = '0' U5-6 = '1'

The adder then adds one bit (LSB) to the coarse data input, as follows:

	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}
Coarse data input	1	1	1	0	1	1	1	1
Carry input from U5-6					1			
Summing input from U5-8	0	0	0	0	0			
Adder Output		1	1	1	1	0		

The modified coarse data output from the adder provides bits 2^{18} - 2^{14} of the output, and the stored fine data provides bits 2^{13} - 2^{1} of the output. The combined data is passed from the board in 18-bit binary parallel format, where bits 2^{18} and 2^{1} represent angular values of 180^{o} and 0.001^{o} respectively.

1.3.6 DUAL OUTPUT REGISTERS BOARD P/N 212194-2

This board contains two separate 24-bit registers fed from a 24-bit data bus. During the azimuth segments of a conversion period, azimuth data is loaded into the appropriate register from the data bus by external control signals. Similarly elevation data is loaded into the elevation register during elevation segments of a conversion period. The register contents are passed as separate 24-bit parallel outputs for use by external binary/BCD conversion circuits.

1.3.6.1 Circuit Description. The 24-bit data input bus is connected to two 24-bit shift registers formed by U1, U4 and U7 (azimuth register) and U2, U5 and U6 (elevation register) (see figure 1-23). 6 bits (A to F) of the 24-bit data input bus are not used (see figure 1-9). The other 18 bits (2^{18} to 2^{1}) represent azimuth or elevation angle information. Control signals at board pins 11, 4, 8 and 6 are passed through inverter stages in U9 to the registers, with relative timing as shown in figure 1-3.

When the SELECT COARSE (AZIMUTH) input goes to logic '1', a logic '0' from U9-4 enables data to be loaded into the azimuth register, on the positive transition of the clock input to the register (negative transition of $\overline{EC}$ at board pin 4). The register then produces the azimuth data outputs from the board.

Similarly the SELECT COARSE (ELEVATION) and $\overline{EC}$ inputs load the 24-bit data into the elevation register, to produce the elevation data outputs from the board.

1.3.7 ADDER/COMPLEMENTER BOARD P/N 212814-1

This board modifies an 18-bit azimuth or elevation data input by an offset value selected by internal switches. The modified 20-bit word, or its complement (inverse), can be selected or passed to the external azimuth or elevation binary/BCD converters.

1.3.7.1 Circuit Description. The 18-bit data input is summed with an 18-bit offset input in an adder, formed by five, 4-bit adders (modules U4-U8) connected in cascade (see figure 1-10). Individual bits of the offset word are held at logic '1' by pull up resistors R1-R18, and can be set to logic '0' by operating OFFSET switches in modules U1-U3.

Individual bits of the adder output are passed to two-input exclusive OR gates in U9-U13. The other gate inputs are held at logic '1' by R21, and can be set to logic '0' by operating a DIRECTION switch in U3. The resultant outputs from the gates are therefore the true adder outputs (DIRECTION switch connected to 0V) or the complement (inverted) adder outputs (DIRECTION switch open).

1.3.8 BINARY/BCD 10^{-3} DECADE BOARD P/N 207733-3 AND BINARY/BCD 10^{2} - 10^{-2} DECADES BOARD P/N 207730-2

These boards operate to convert 17 bits of an 18-bit offset binary input into a five decade BCD format suitable for driving external 7-segment displays. The binary input represents angle data in the range 0° to 359.999° with a resolution of 0.001°. The BCD output represents angle data in the range 0° to 359.99° with a resolution of 0.01°. A 'round-off' facility is available but is not used.

1.3.8.1 Block Diagram Description. The 17-bit offset binary input (LSB not used) is divided into two binary groups comprising bits 2^{2} - 2^{13} and 2^{4} - 2^{18} (see figure 1-11). Bits 2^{2} -2^{13} are applied to a decade circuit (10^{3}), bits 2^{4} - 2^{18} are further divided and applied to their respective decade circuits (10^{2} - 10^{-2}). Each decade circuit consists of cascaded 4-bit full adders and a binary-to-BCD converter stage. The angular values of individual bits in the binary input are as follows:

BIT	VALUE	
18 (MSB)	180.000°	
17	90.000°	
16	45.000°	
15	22.500°	
14	11.250°	
13	5.625°	
12	2.812°	
11	1.406°	
10	0.703°	
9	0.351°	
8	0.175°	
7	0.087°	
6	0.043°	
5	0.021°	
4	0.010°	
3	0.005°	
2	0.002°	
1 (LSB)	0.001°	(Not used)

The relationship between the binary input data and the configuration of the decade circuits provides a resultant mathematical output where the MSB represents 200^{o} and the LSB represents 0.01^{o}. For example, an angle of 237.546^{o} is represented by a data input as follows:

INPUT BIT	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
LOGIC LEVEL	1	0	1	0	1	0	0	0	1	1	1	0	1	1	0	0	1	0

The resultant output logic levels from the five decade circuits are as follows:

	10^{2} Decade		10^{1} Decade				10^{0} Decade			
VALUE	200^{o}	100^{o}	80^{o}	40^{o}	20^{o}	10^{o}	8^{o}	4^{o}	2^{o}	1^{o}
LOGIC LEVEL	'1'	'0'	'0'	'0'	'1'	'1'	'0'	'1'	'1'	'1'

	10^{-1} Decade				10^{-2} Decade			
VALUE	0.8^{o}	0.4^{o}	0.2^{o}	0.1^{o}	0.08^{o}	0.04^{o}	0.02^{o}	0.01^{o}
LOGIC LEVEL	'0'	'1'	'0'	'1'	'0'	'1'	'0'	'0'

1.3.8.2 Circuit Description. The following circuit description is written around the quoted binary input data of 237.546^{o} (see paragraph 1.3.8.1).

a. The 10^{-3} decade circuit consists of 4-bit full adders U1-U6 and binary-to-BCD converter U14 (See figure 1-12). Input and output logic levels for each adder are as follows:

Adder U1					
'A' inputs		0	1	0	1
'B' inputs		0	0	1	0
Carry input					1
Carry and Sum outputs	0	1	0	0	0
Adder U2					
'A' inputs		0	0	0	0
'B' inputs		0	0	0	0
Carry input					1
Carry and Sum outputs	0	0	0	0	1
Adder U3					
'A' inputs		0	0	0	1
'B' inputs		1	0	0	0
Carry input					0
Carry and Sum outputs	0	1	0	0	1
Adder U4					
'A' inputs		1	0	0	1
'B' inputs		0	0	0	1
Carry input					0
Carry and Sum outputs	0	1	0	1	0

Adder U5					
'A' inputs		1	0	1	0
'B' inputs		0	1	1	0
Carry input					0
Carry and Sum outputs	1	0	0	0	0
Adder U6					
'A' inputs		1	0	0	0
'B' inputs		0	0	0	0
Carry input					0
Carry and Sum outputs	0	1	0	0	0

The carry and sum outputs from adder U6 are passed through non-inverting buffer gates (U7) to binary-BCD converter (U14) which produces a BCD output as follows:

Y6	Y5	Y4	Y3	Y2	Y1	(LSB)
0	0	1	0	1	1	

The LSB output from U5-10 is added as an LSB to U14 output, to give a BCD output from the board, as follows:

(0.04)	(0.02)	(0.01)	(0.008)	(0.004)	(0.002)	(0.001)
0	0	1	0	1	1	0

The 0.04, 0.02 and 0.01 outputs provide carry inputs to the 10^{-2} decade. The remaining four outputs provide the 10^{-3} decade BCD output at board pins C, D, 4 and K.

b. The 10^{-2} decade circuit consists of 4-bit full adders A1-A4 and binary-BCD converter A6 (see figure 1-13). Input and output logic levels for each adder are as follows:

Adder A1					
'A' inputs		0	1	1	1
'B' inputs		0	1	1	1
Carry input					0
Carry and Sum outputs	0	1	1	1	0
Adder A2					
'A' inputs		0	1	1	0
'B' inputs		0	1	0	1
Carry input					0
Carry and Sum outputs	0	1	0	1	1
Adder A3					
'A' inputs		1	0	1	1
'B' inputs		1	0	0	1
Carry input					1
Carry and Sum outputs	1	0	1	0	1

Adder A4					
'A' inputs		0	1	0	1
'B' inputs		0	0	0	1
Carry input					0
Carry and Sum outputs	0	0	1	1	0

The carry and sum outputs of adder A4, and the output from A3-11 are passed through non-inverting buffers (A5) to binary-BCD converter (A6) which produces a 6-bit BCD output as follows:

Y6	Y5	Y4	Y3	Y2	Y1	(LSB)
0	1	0	0	1	0	

The LSB output from A3-10 is added as an LSB to A6 output, to give a BCD output as follows:

(0.4)	(0.2)	(0.1)	(0.08)	(0.04)	(0.02)	(0.01)
0	1	0	0	1	0	1

The 0.4, 0.2 and 0.1 outputs provide carry inputs to the 10^{-1} decade. The remaining four outputs provide the 10^{-2} decade BCD output at board pins 8, 9, 10 and 11. (The fourth CARRY input via board pin 17 is normally part of the 'round-off' operation).

c. The 10^{-1} decade input consists of 4-bit full adders A8-A11 and binary-BCD converter A13. Input and output logic levels for each adder are as follows:

Adder A8					
'A' inputs		0	1	1	1
'B' inputs		0	0	1	0
Carry input					1
Carry and Sum outputs	0	1	0	1	0
Adder A9					
'A' inputs		1	0	1	0
'B' inputs		0	0	0	0
Carry input					1
Carry and Sum outputs	0	1	0	1	1
Adder A10					
'A' inputs		1	0	1	1
'B' inputs		0	0	0	0
Carry input					0
Carry and Sum outputs	0	1	0	1	1
Adder 11					
'A' inputs		0	1	0	1
'B' inputs		0	0	0	1
Carry input					1
Carry and Sum outputs	0	0	1	1	1

The carry and sum outputs of adder A11 are passed through non-inverting buffers (A12) to binary-BCD converter A13 which produces a 6 bit BCD output as follows:

Y6	Y5	Y4	Y3	Y2	Y1	(LSB)
0	0	1	0	1	0	

The LSB output from A10-10 is added as an LSB to A13 output to give a BCD output as follows:

(4)	(2)	(1)	(0.8)	(0.4)	(0.2)	(0.1)
0	0	1	0	1	0	1

The 4, 2 and 1 outputs provide carry inputs to the 10^0 decade. The remaining four outputs provide the 10^{-1} decade BCD output at board pins 5, 6, 7 and J. (The fourth CARRY input via board pin 16 is normally part of the 'round-off' operation).

d. Tune 10^0 decade circuit consists of 4-bit full adders A15, A16 and binary-BCD converter A18. Input and logic output levels for each adder are as follows:

Adder A15					
'A' inputs		0	0	0	0
'B' inputs		0	1	0	1
Carry input					1
Carry and Sum outputs	0	0	1	1	0
Adder A16					
'A' inputs		0	1	1	0
'B' inputs		0	0	0	0
Carry input					1
Carry and Sum outputs	0	0	1	1	1

The carry and sum outputs of adder A16 are passed through non-inverting buffers (A17) to binary-BCD converter (A18) which produces a BCD output as follows:

Y5	Y4	Y3	Y2	Y1	(LSB)
0	0	0	1	1	

The LSB output from A16-10 is added as an LSB to A18 output to give a BCD output as follows:

(20)	(10)	(8)	(4)	(2)	(1)
0	0	0	1	1	1

The 20 and 10 outputs provide carry inputs to the 10^1 decade. The remaining four outputs provide the 10^0 decade BCD output at board pins S,14,13 and U.

e. The 10^1 decade circuit consists of a 4-bit full adder A7 and binary-to-BCD converter A21. Input and output logic levels for the adder are as follows:

Adder A7

'A' inputs		1	0	0	1
'B' inputs		0	1	0	0
Carry input					0
Carry and Sum outputs	0	1	1	0	1

The carry and sum outputs of adder A7 are passed through non-inverting buffers (A14) to binary-to-BCD converter (A21) which produces a BCD output as follows:

Y5	Y4	Y3	Y2	Y1	(LSB)
0	1	0	0	1	

The LSB output from A7-10 is added as an LSB to A14 output to give a BCD output as follows:

(200)	(100)	(80)	(40)	(20)	(10)
0	1	0	0	1	1

The 200 and 100 outputs provide carry inputs to the 10^2 decade. The remaining four outputs provide the 10^1 decade BCD output at board pins 2,3,4 and B.

f. The 10^2 decade circuit consists of 2-bit full adder A20. Input and output logic levels for the adder are as follows:

Adder A20

A inputs		0	1	
B inputs		0	1	
Carry input			0	
Carry and Sum outputs	0	1	0	

The sum outputs of adder A20 provide the 10^2 decade BCD outputs at board pins D and H, where a logic '1' at board pin D represents 200. Any carry generated by this circuit is redundant and not used.

The outputs from the 10^{-3} decade are applied to binary-BCD converter A19 to produce a CARRY output at board pin P. This output is logic '0' when the 10^{-3} output represents 0.000 to 0.004 and logic '1' when the 10^{-3} output represents 0.005 to 0.009. If the CARRY output is connected to the CARRY inputs at board pins 16 and 17, the last digit of the final BCD output is 'rounded-off'.

1.3.9 DIFFERENTIAL LINE DRIVER BOARD P/N 212815-1

This board converts each bit of a 22-bit parallel data input into a differential output at TTL levels.

1.3.9.1 Circuit Description. The circuit consists of 11 identical modules (U1-U11) containing a dual differential line driver circuit suitable for driving balanced output lines with high power dissipation at normal line impedance (see figure 1-14). Four boards are used in the angle encoder unit (A11, A12, A16 and A17) to handle binary or BCD azimuth or elevation data. Table 1-1 provides a cross reference between the input signal name shown on the schematic diagram and the signal used in each application.

Table 1-1 Differential Line Driver Inputs

Signal Input	A11 BCD Azimuth	A12 and A16 Binary azimuth and elevation	A17 BCD elevation
Bit 18	200	Bit 18	200
Bit 17	100	Bit 17	100
Bit 16	80	Bit 16	80
Bit 15	40	Bit 15	40
Bit 14	20	Bit 14	20
Bit 13	10	Bit 13	10
Bit 12	8	Bit 12	8
Bit 11	4	Bit 11	4
Bit 10	2	Bit 10	2
Bit 9	1	Bit 9	1
Bit 8	0.8	Bit 8	0.8
Bit 7	0.4	Bit 7	0.4
Bit 6	0.2	Bit 6	0.2
Bit 5	0.1	Bit 5	0.1
Bit 4	0.08	Bit 4	0.08
Bit 3	0.04	Bit 3	0.04
Bit 2	0.02	Bit 2	0.02
Bit 1	0.01	Bit 1	0.01
A	Az Reg Update	Not used	El Reg Update
B	0.008	Not used	0.008
C	0.004	Not used	0.004
D	0.002	Not used	0.002

1.3.10 1200 Hz OSCILLATOR BOARD P/N 211190-5

The function of this board is to generate a 1200 Hz reference sinewave for external equipment.

1.3.10.1 Circuit Description. U3 and associated components form a high Q active-filter stage with a resonant frequency of 1200 Hz ± 240 Hz (see figure 1-15). At this frequency the filter produces an output pulse of approximate amplitude 10 V p-p. This pulse is passed to output stage U1, and to a feed-back stage U2. U2 is a unity gain inverter, and passes the pulse as positive feedback to U3 inverting input to maintain oscillations. Back-to-back zener diodes CR2 and CR1 form a 'soft clipper', limiting the amplitude of the signal fed back to U3. These diodes also shape the signal to form an approximate sinewave, reducing waveform distortion. R3 is selected on test to set the amplitude of the output waveform.

Output amplifier U1 is a unity gain stage with high current output capability (approximately 1A). Resistors R1 and R2 are connected in the amplifier dc supply lines to provide current limiting. The amplifier output provides a reference output at pins 8 and J of 3.7 V rms (nominal), and is coupled through C2 and C1 to step-up (1:3) transformer T1. The output from T1 secondary provides a 12 V rms (nominal) 1200 Hz output between pins 20 (X) and 21 (Y).

1.3.11 ± 15 VDC POWER SUPPLY ASSEMBLY-R115

The power supply produces stable +15 and -15 volts dc, at 0.75 A from a 115 Vac input supply.

1.3.11.1 Circuit Description. The input circuit consists of transformer T1 with thermal cut-out protection at 82°C provided by S1 at the primary winding (see figure 1-16). A secondary winding, centre-tapped to provide a common output rail, feeds a full-wave bridge rectifier circuit D1 to D4 which produces raw positive and negative dc voltages smoothed by C1 and C2. Zener diode Z1 and transistor Q4 forms a voltage divider to produce a reference voltage of 14.4 V applied to A1/8 and A2/8 and 7. Zener diode Z2 provides a +7.5 V reference voltage to A1/6 and A2/10 and 1. This ensures stable operation of A1 and A2 independent of changes in output voltage.

Integrated circuit A1 compensates for positive output load variations. Potentiometer P1 is set to provide the required positive output voltage. Regulation within A1 via A1-7, controls the base of Q2. Transistor Q2, in turn, controls the base of Q1 to maintain the set voltage level on the positive rail. Any variations of output load that may occur will now produce a voltage change at the junction of divider network P1, R9 and R20. This 'sensed' voltage is applied to the inverting input at A1-2. Filter C3, R10 ensures a ripple-free input to A1-2.

A reference voltage, generated within A1, is resistively coupled to A1-3 (non-inverting input). The resultant output at A1-7 is an inversion of the dc input applied to A1-2. This inverted output controls conduction of Q2 and Q1 to restore the dc output to the level set by P1. Further stability of operation is achieved by the frequency compensation circuit of C5 and R16 applied to A1-9. Resistors R1 and R2 provide the bias for Q2. Final output smoothing is effected by capacitor C8. Diode D6 acts as a positive output polarity reversal protection and protects the regulators during 'start-up'. LED SI-1, with its current limit resistor R31, provides an 'output available' indication.

The series output resistor R6 senses the current drawn by the positive output load. The current limit transistor Q3 is normally held cut-off by the divider network of resistors R4, R5 and R7, R8. An increase in load current beyond 0.75 A will cause a sufficient drop in potential at the base of Q3 and Q3 conducts. The subsequent rise in potential at A1-10 produces an increase of voltage at A1-7, reducing the drive to Q2 and Q1 and reducing output current to a safe value.

Integrated circuit A2 compensates for negative output load variations and acts in a similar manner to the positive voltage regulation. Potentiometer P2 is set to provide the required negative output voltage and regulation of the negative rail is effected by Q7 and Q6. Any variations occurring in the output load will produce a voltage change at the junction of R23 and R14 and A2-3 (non-inverting input). The voltage reference, at A2-4, is not connected. A voltage reference derived from the positive divider network junction R24 and R15, is applied to A2-2 (inverting input). The resultant inverse dc output on A2-6 is applied to the emitter of Q5. Q5 acts as a driver, with its base tied to zener voltage Z2, to vary conduction of Q7 and Q6 and restore the set negative level of output.

The series output resistor R30 senses the current drawn by the negative output load. Current limit transistor Q8 is normally cut-off by the divider chain R29, R28. When current drawn exceeds 0.75 A, a sufficient rise in potential at the junction of R29 and R28 causes Q8 to conduct. The consequent voltage drop across R25 produces a negative potential at A2-1. A resultant drop in output from A2-6 reduces the drive via Q5, Q7 and Q8 to Q6 and reduces the output current to a safe value. Frequency compensation and ripple free inputs to A2 are provided by C4, C7 and C10. Diode D7 provides negative output polarity reversed protection.

1.3.12 5 VDC POWER SUPPLY ASSEMBLY - 210

The power supply is a 20 kHz pulse-width modulated converter which provides a stable dc output in the range +3.5 V to +5.5 V from a nominal ac mains supply input of 115 V, 60 Hz. Maximum ripple is 25 mV p-p and the maximum current rating is preset to 10 A.

Suitable protection circuits are provided for overvoltage, overcurrent and overtemperature conditions. RFI suppression is included at all inputs and outputs and special protection is provided against excessive mains supply surges.

Pulse width control is achieved by means of a magnetic amplifier which controls the on/off time of a non-saturating power inverter.

WARNING

'Soft' overvoltage protection is used (i.e. not 'crowbar' type) and parallel connection of the power supply is not possible.

1.3.12.1 Circuit Description. The 115 Vac mains supply input on connectors L1 and L2 is applied to the main rectifier (D1-D4) via an RFI filter (C14, C15, L6, L7, C21, C22), an inrush current limiting resistor (R1) and a thermostat (S1) (see figure 1-17). The thermostat provides overtemperature protection for the power supply components and disconnects the neutral line when the internal temperature exceeds $82^{o} \pm 2.8^{o}C$.

NOTE

Resistor R1 should not be replaced by any component other than that specified in the components list.

The main rectifier produces an unregulated 180 Vdc supply which is filtered by C1 to provide a high voltage supply for the power inverter. Z5 is a 'transorb' component which limits this supply to approximately 200 V in the event of an excessive mains supply surge.

An oscillator circuit formed by Q2, Q3, T1 is free-running and acts as a dc/ac inverter which provides the basic switching function. At switch-on, an initial dc supply of approximately +16.8 V is applied via D5 to the emitters of Q2, Q3 by a voltage source comprising zener diode Z1 and emitter-follower Q1. Zener diode Z4 and potential divider R5, R6 provide a dc supply of approximately +16 V to the oscillator base drive winding (pins 4, 5, 6 of T1).

A few milliseconds after switch-on, an oscillator dc supply of +22 V is provided by the full-wave rectified and filtered output (D6, D7, C2) of a secondary winding on transformer T2 (pins 1, 2, 3). This voltage also reverse-biases diode D5 and the initial starting voltage is therefore isolated. The oscillator is started by bleed current flowing through R5 from the dc supply and providing base current for both Q2 and Q3. The one with the best gain (say Q2) tends to conduct first and, since the primary winding (pins 1, 2, 3) and the base drive winding (pins 4, 5, 6) of T1 are connected in a regenerative configuration, switches on fast and Q3 is switched hard off. Q2 stays on for a time determined by the action of Q2, Q3 and T1.

T1 is designed to saturate and when this occurs the primary winding inductance falls to a low level and causes a rapid increase in Q2 collector current. The corresponding rise in voltage across the transistor, which reduces drive to the base via the drive winding, further increases the voltage rise and results in a fast regenerative switch-off for Q2. The stored magnetic energy in T1 reverses the voltages on the windings and causes Q3 to switch on fast. When Q3 switches off again, the cycle of operation is repeated and the resultant output is a unity mark/space ratio square wave whose amplitude is twice that of the oscillator dc supply.

With the oscillator operating, zener diode Z4 becomes forward-biased and, in conjunction with resistor R6, provides a low impedance base source for Q2 and Q3. Series network C3, R4 provides damping for the primary winding and prevents spurious oscillations and switching 'spikes'.

Transistors Q4, Q5 and step-down transformer T2 form a non-saturating power inverter. The relative on/off timing of the transistors which determines the final output is controlled by a magnetic amplifier (MA1). Transistors Q4 and Q5 are switched by the outputs of two anti-phase secondary windings of T1 (pins 7, 8 and pins 10, 9 respectively) which are driven by the square wave output of the 20 kHz oscillator. Assume, initially, that Q4 is switched on. Current is drawn from the positive switching supply rail and fed through the primary winding of T2 such that pin 4 is more positive than pin 5. When Q4 switches off again, there is a short delay (dead band) and then Q5 is switched on. In this case current is drawn through T2 primary winding such that pin 5 is now more positive than pin 4. Thus the switching of Q4 and Q5 produces an alternating waveform in T2 primary with a mark/space ratio determined by the transistor conduction times.

The 'dead band' ensures that the conduction times do not overlap, protection for Q4 and Q5 against excessive reverse voltages is provided by diodes D22 and D23 respectively. For setting-up purposes the conduction time of Q5 can be preset by P1 to match that of Q4. The range of control is approximately 16 $\pm$ 3uSec.

A centre-tapped step down secondary winding on T2 (pins 6, 7, 8) provides the final output which is full-wave rectified by D17 and D18, then filtered by L1, L2, L3, L8 and their associated components. Capacitors C16, C17 form an RFI filter. Bleed resistor R20 provides loading when no external load is connected to the +5 and -5 V output terminals.

Magnetic amplifier (MA1) varies the duty cycle of the power inverter and the regulation of the output voltage. There are three control inputs to the magnetic amplifier, the main input coming from the voltage sense amplifier to provide output voltage regulation. A second input is provided by the overcurrent sense amplifier and the third input is provided by the overvoltage sense circuit.

Voltage sense amplifier (Q8-Q10) monitors the power supply output via the sense lines, and sets and maintains the output at the required level. The output fed to the (+) SENS and (-) SENS terminals, via the local sense links, is passed through an RFI filter (C28, C30, L9, L10, C25, C29) and applied to a potential divider network comprising D16, P2 (the preset 5 V ADJ control) and R29. D16 provides temperature compensation and a sample of the output is picked off by the wiper of P2. A comparator (Q10) compares the sample with the +3.3 V reference voltage (set by zener diode Z3) and produces an output to control a two-stage drive amplifier (Q9, Q8). The frequency response of the two-stage amplifier is determined by feedback network C11, R23 and C7. The output from Q8 is applied via R21 to a control winding (pins 4 and 3) of the magnetic amplifier MA1 to form a closed loop in which detected changes in the output are corrected via the power inverter.

Overcurrent sense amplifier (Q6, Q7) detects overcurrent conditions by monitoring the voltage drop across inductor L1 in the positive output line. The normal output voltage is restored when the overcurrent condition disappears. A secondary winding on T2 (pins 9 and 10), together with diode D14 and filter capacitor C8, provide an additional positive power supply rail for the overcurrent control circuit, this supply being referenced to the positive output rail via clamping diode D15.

Transistors Q6 and Q7 form a differential amplifier in which the base of Q6 is held at a reference level set by a resistive network comprising R15, R19, R33, R34, thermistor R35 and preset P3. Normally Q6 is on and Q7 is off but during overcurrent conditions the voltage drop across L1 makes Q7 base more negative than the reference voltage. Thus Q7 switches on and provides an additional input to the output voltage control winding (pins 4 and 3) of the magnetic amplifier MA1. The point at which this occurs is normally set (by P3) to be 140% of the normal output current rating. Diode D12 is included to provide temperature compensation.

Overvoltage sensing is not of the usual 'crowbar' type since there is no series-pass element to protect against short-circuiting. A short-circuited transistor in this power supply results in no output voltage rather than an overvoltage condition. In the event of a failure in the voltage sense amplifier a sample output of the voltage is fed via zener diode Z2 and resistor R17 to a control winding (pins 6 and 5) of the magnetic amplifier MA1 to limit the output voltage at +6.8 V to +7 V maximum.

1.3.13 EXTENDER BOARD P/N 212189-1

The 80-way extender board enables the following boards of the angle encoder unit to be functionally tested:

a. Synchronous Demodulator/Multiplexer Board P/N 212195-6

b. Signal Conditioning Board P/N 206497-13

c. Sin/Cos Network Board P/N 206499-1

d. Successive Approximation Board P/N 206498-1

e. Address/Combination Board P/N 209508-1

f. Binary/BCD 10^{2} to 10^{-2} Decades Board P/N 207730-2

g. Binary/BCD 10^{-3} Decade Board P/N 207733-3

h. 1200 Hz Oscillator Board P/N 211190-5

1.3.14 50-WAY EXTENDER BOARD P/N 211300-1

The 50-way extender board enables the following boards of the angle encoder unit to be functionally tested:

a. Dual Output Register Board P/N 212194-2

b. Adder Complementer Board P/N 212814-1

c. Differential Line Driver Board P/N 212815-1

1.4 INTEGRATED CIRCUIT DATA

Table 1-2 lists the integrated circuits used in the LRU's of the angle encoder unit.

Table 1-2 Integrated Circuit Data

Circuit Ref	Description	Figure Reference
SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD		
U1, U2, U3, U4, U5, U6, U7, U8, U10, U12, U13, U15,	UA741	1-58
U9.	LM118	1-56
U11, U14.	H12-200	1-59
SIGNAL CONDITIONING BOARD		
A2, A5.	UA741	1-58
A3, A6.	LM101A	1-33
A4, A7.	UA709	1-57
SIN/COS NETWORK BOARD		
A1	UA709	1-57
SUCCESSIVE APPROXIMATION BOARD		
U1, U3, U4.	CD4049	1-50
U2	MC14559	1-62
U5	MC14549	1-62
U6	CD4027	1-48
U7, U9, U12, U14, U16.	SN54136	1-38
U8	898-1-R	1-61
U10	CD4011	1-49
U11	SN5474	1-46
U13, U15, U17.	SN5404J	1-34
ADDRESS/COMBINATION BOARD		
U1, U5, U6.	SN7404J	1-34
U2	SN7400	1-47
U3, U9, U12.	74LS138	1-35
U4	SN74177	1-39
U7	NE555	1-45
U8	SN74121	1-41
U10, U11	SN74LS10	1-42
U13, U16, U17, U18.	SN74178	1-40
U14	SN7482	1-52
U15	SN7483	1-53

Table 1-2 Integrated Circuit Data (Continued)

Circuit Ref	Description	Figure Reference
DUAL OUTPUT REGISTER BOARD		
U1, U2, U4, U5, U7, U8.	54LS377	1-37
U9	54LS04	1-55
BINARY/BCD 10^{-2} TO 10^{-2} DECADES BOARD		
U1, U2, U3, U4, U7, U8	CD4008A	1-54
U9, U10, U11, U15, U16.		
U5, U12, U14, U17.	CD4010A	1-60
U6, U13, U18, U19, U21.	SN74185A	1-36
U20	SN7482	1-52
BINARY/BCD 10^{-3} DECADE BOARD		
U1-U6.	CD4008A	1-54
U7	CD4010A	1-60
U14	SN54185	1-36
DIFFENTIAL LINE DRIVER BOARD		
U1-U11.	SN75183	1-44
1200 Hz OSCILLATOR POWER SUPPLY BOARD		
U1	LH0021C	1-63
U2, U3.	LM101A	1-33

PART 1

SECTION II

MECHANICAL DESCRIPTION

1.5 GENERAL

This section provides a description of the mechanical construction of each LRU within the angle encoder unit.

1.6 MECHANICAL DESCRIPTION

The following paragraphs describe each LRU referenced to individual figures showing component location, test points and preset controls. Pin assignment tables for each LRU are listed in tables 1-3 to 1-13.

1.6.1 SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of each board. Figure 1-18 indicates component location, test points E1-E10 and the 'amplifier-offset' resistors.

Table 1-3 Synchronous Demodulator/Multiplexer Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A		1	
B	-15 Vdc	2	-15 Vdc
C	+15 Vdc	3	+15 Vdc
D		4	
E	Fine Azimuth/Elevation Cos (LO)	5	Fine Azimuth/Elevation Cos (HI)
F	1.2 kHz Reference	6	Select Fine Azimuth/Elevation
H	Fine Sin Azimuth/ Elevation Sin (LO)	7	
J	MPLX Cos	8	MPLX Sin
K		9	
L		10	
M		11	
N		12	
P	Fine Azimuth Elevation Sin (HI)	13	
R	Ref SQ. Out	14	
S	Coarse Azimuth/ Elevation Cos (LO)	15	

Table 1-3 Synchronous Demodulator/Multiplexer Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
T	Coarse Azimuth/ Elevation Cos (HI)	16	Elev Cos dc Out
U		17	
V		18	
W	Gnd	19	Gnd
X		20	
Y	Select Coarse Azimuth/Elevation	21	
z		22	
AA	+5 Vdc	23	+5 Vdc
BB	Coarse Azimuth/ Elevation Sin (LO)	24	
CC	Coarse Azimuth/ Elevation Sin (HI)	25	

1.6.2 SIGNAL CONDITIONING BOARD P/N 206497-13

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. Figure 1-19 indicates component location, four adjustment potentiometers R15, R26, R36, R47 and six 'select-at-test' (SAT) resistors R10, R12, R31, R32, R52 and R53.

Table 1-4 Signal Conditioning Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 Vdc
B	-15 Vdc	2	-15 Vdc
C	+15 Vdc	3	+15 Vdc
D	Cos Pol	4	
E	Cos Cont	5	Sin Pol
F		6	
H	Sin Cont	7	
J	Test Point	8	
K	Test Point	9	
L		10	Clock
M	Cos	11	Cos
N		12	
P		13	
R	Sin	14	Sin
S		15	
T		16	
U		17	
V		18	

Table 1-4 Signal Conditioning Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
W	Sig gnd	19	Sig Gnd
X	MPLX Sin	20	
Y	MPLX Cos	21	EC
Z		22	
AA		23	
BB		24	
CC	Gnd	25	Gnd

1.6.3 SIN/COS NETWORK BOARD P/N 206499-1

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. The component location diagram (figure 1-20) indicates the single adjustment potentiometer R31.

Table 1-5 Sin/Cos Network Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 Vdc
B	-15 Vdc	2	-15 Vdc
C	+15 Vdc	3	+15 Vdc
D		4	$2^{1}X$
E		5	$2^{2}X$
F		6	$2^{12}X$
H		7	$2^{3}X$
J		8	$2^{4}X$
K		9	$2^{5}X$
L		10	$2^{6}X$
M	Cos	11	Cos
N		12	$2^{7}X$
P		13	$2^{8}X$
R	Sin	14	Sin
S		15	$2^{9}X$
T		16	$2^{10}X$
U		17	$2^{11}X$
V		18	Test Point
W	Sig Gnd	19	Sig Gnd
X	E	20	Comp Out
Y	D	21	
Z		22	
AA	C	23	
BB	B	24	A
CC	Gnd	25	Gnd

1.6.4 SUCCESSIVE APPROXIMATION BOARD P/N 206498-1

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. No alignment or adjustment components are fitted to this pcb. For component location refer to figure 1-21.

Table 1-6 Successive Approximation Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 Vdc
B	Sin Cont	2	Sin Pol
C	Cos Cont	3	Cos Pol
D	2^{13}	4	2^{12}
E	EC	5	2^{11}
F	2^{10}	6	E
H		7	SC
J	$2^{\overline{12}}$	8	Clock
K		9	EC
L	2^{9}	10	Uni-Clock
M		11	2^{8}
N		12	2^{7}
P	$2^{9}X$	13	$2^{11}X$
R	$2^{8}X$	14	$2^{10}X$
S		15	C
T	B	16	D
U	$2^{7}X$	17	A
V	$2^{4}X$	18	$2^{6}X$
W	2^{4}	19	$2^{5}X$
X	2^{6}	20	2^{5}
Y		21	2^{1}
Z	Comp Out	22	2^{3}
AA	$2^{3}X$	23	2^{2}
BB	$2^{2}X$	24	$2^{1}X$
CC	Gnd	25	Gnd

1.6.5 ADDRESS/COMBINATION BOARD P/N 209508-1

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. Figure 1-22 indicates component location and one SAT resistor R1.

Table 1-7 Address/Combination Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 V
B	Comb Data Output 2^1		Conv Data Input 2^1
C		3	
D	Comb Data Output 2^2	4	Comb Data Output 2^3
E	Conv Data Input 2^2	5	Conv Data Input 2^3
F	$\overline{EC}$	6	Comb Data Output 2^5
H	Comb Data Output 2^4	7	Conv Data Input 2^5
J	Conv Data Input 2^4	8	Conv Data Input 2^6
K	Comb Data Output 2^7	9	Comb Data Output 2^6
L	Comb Data Output 2^9	10	EC
M	Comb Data Output 2^8	11	Conv Data Input 2^7
N	Conv Data Input 2^8	12	Select Coarse (Elevation)
P	Comb Data Output 2^{14}	13	Conv Data Input 2^9
R	Comb Data Output 2^{17}	14	Conv Data Input 2^{12}
S	Conv Data Input 2^{10}	15	Comb Data Output 2^{15}
T	Conv Data Input 2^{11}	16	Comb Data Output 2^{16}
U	SC	17	Comb Data Output 2^{12}
V	Comb Data Output 2^{13}	18	Conv Data Input 2^{13}
W	Comb Data Output 2^{11}	19	Comb Data Output 2^{18}
X	Comb Data Output 2^{10}	20	Select Fine (Azimuth)
Y	Stop Clock	21	Select Coarse (Azimuth)
Z	EL Reg Update	22	AZ Reg Update
AA	AZ Data Ready	23	Conv Comp
BB	Gnd	24	Gnd
CC	Select Fine (Elevation)	25	EL Data Ready

1.6.6 DUAL OUTPUT REGISTERS BOARD P/N 212194-2

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 80 edge-pins which form the lower edge of the board. No alignment or adjustment components are fitted to this pcb. For component location refer to figure 1-23.

Table 1-8 Dual Output Registers Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
1	+5 Vdc	2	$\underline{+5}$ Vdc
3	Elevation Data Output (Bit 3)	4	$\overline{EC}$
5	Data Input Bus (Bit 3)	6	EC
7	Elevation Data Output (Bit 4)	8	Select Coarse Elevation
9	Elevation Data Output (Bit 5)	12	Elevation Data Output (Bit 6)
11	Select Coarse (Azimuth)	10	Elevation Data Output (Bit 8)

Table 1-8 Dual Output Registers Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
	Elevation Data Output (Bit 7)	14	Azimuth Data Output (Bit 5)
15	Elevation Data Output (Bit 9)	16	Azimuth Data Output (Bit 9)
17	Elevation Data Output (Bit 10)	18	Azimuth Data Output (Bit 7)
19	Azimuth Data Output (Bit 3)	20	Elevation Data Output (Bit E)
21	Azimuth Data Output (Bit 4)	22	Elevation Data Output (Bit D)
23	Azimuth Data Output (Bit 6)	24	Elevation Data Output (Bit 2)
25	Azimuth Data Output (Bit 10)	26	Elevation Data Output (Bit 1)
27	Azimuth Data Output (Bit 8)	28	Elevation Data Output (Bit A)
29	Elevation Data Output (Bit C)	30	Data Input Bus (Bit 5)
31	Elevation Data Output (Bit F)	32	Data Input Bus (Bit 8)
33	Elevation Data Output (Bit B)	34	Data Input Bus (Bit 7)
35	Data Input Bus (Bit 4)	36	Azimuth Data Output (Bit D)
37	Azimuth Data Output (Bit C)	38	Azimuth Data Output (Bit E)
39	Data Input Bus (Bit 9)	40	Azimuth Data Output (Bit F)
41	Data Input Bus (Bit 10)	42	Elevation Data Output (Bit 12)
43	Data Input Bus (Bit 6)	44	Elevation Data Output (Bit 13)
45	Azimuth Data Output (Bit B)	46	Elevation Data Output (Bit 14)
47	Azimuth Data Output (Bit 1)	48	Data Input Bus (Bit B)
49	Azimuth Data Output (Bit 2)	50	Data Input Bus (Bit E)
51	Elevation Data Output (Bit 11)	52	Data Input Bus (Bit 1)
53	Data Input Bus (Bit C)	54	Data Input Bus (Bit 2)
55	Data Input Bus (Bit A)	56	Data Input Bus (Bit F)
57	Data Input Bus (Bit D)	58	Elevation Data Output (Bit 16)
59	Azimuth Data Output (Bit A)	60	Elevation Data Output (Bit 17)
61	Elevation Data Output (Bit 15)	62	Elevation Data Output (Bit 18)
63	Azimuth Data Output (Bit 14)	64	Azimuth Data Output (Bit 13)
65	Data Input Bus (Bit 15)	66	Data Input Bus (Bit 13)
67	Azimuth Data Output (Bit 15)	68	Data Input Bus (Bit 14)
69	Data Input Bus (Bit 16)	70	Azimuth Data Output (Bit 12)

Table 1-8 Dual Output Registers Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
71	Azimuth Data Output (Bit 16)	72	Data Input Bus (Bit 12)
73	Azimuth Data Output (Bit 17)	74	Data Input Bus (Bit 11)
75	Data Input Bus (Bit 17)	76	Azimuth Data Output (Bit 11)
77	Logic Ground	78	Logic Ground
79	Data Input Bus (Bit 18)	80	Azimuth Data Output (Bit 18)

1.6.7 ADDER/COMPLEMENTER BOARD P/N 212814-1

This LRU is a identical rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 80 edge-pins which form the lower edge of the board. Figure 1-24 indicates component location and location of the offset switches (20 off) and the direction switch.

Table 1-9 Adder/Complementer Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
1	+5 Vdc	2	+5 Vdc
3	Data Input A	4	
5	Az/Elev Data Input (Bit 1)	6	
7		8	
9		10	
11	Offset Binary Output 2	12	
13	Offset Binary Output 1 (LSB)	14	
15	Az/Elev Data Input (Bit 2)	16	
17	Data Input B	18	
19	Az/Elev Data Input (Bit 4)	20	
21	Az/Elev Data Input (Bit 5)	22	
23	Offset Binary Output 3	24	
25	Offset Binary Output 4	26	
27	Az/Elev Data Input (Bit 3)	28	
29	Offset Binary Output 5	30	
31	Offset Binary Output 6	32	
33	Az/Elev Data Input (Bit 6)	34	
35	Az/Elev Data Input (Bit 8)	36	
37	Az/Elev Data Input (Bit 9)	38	
39		40	
41		42	
43	Offset Binary Output 7	44	
45	Offset Binary Output 8	46	
47	Offset Binary Output 9	48	
49	Offset Binary Output 10	50	

Table 1-9 Adder/Complementer Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
51		52	
53	Az/Elev Data Input (Bit 10)	54	
55	Az/Elev Data Input (Bit 7)	56	
57	Az/Elev Data Input (Bit 12)	58	
59	Az/Elev Data Input (Bit 13)	60	
61	Offset Binary Output 11	62	
63	Offset Binary Output 12	64	
65	Offset Binary Output 13	66	Az/Elev Data Input (Bit 14)
67	Offset Binary Output 14	68	Az/Elev Data Input (Bit 11)
69	Offset Binary Output 15	70	Az/Elev Data Input (Bit 16)
71	Offset Binary Output 16	72	Az/Elev Data Input (Bit 17)
73	Offset Binary Output 17	74	Az/Elev Data Input (Bit 18)
75	Offset Binary	76	Az/Elev Data Input (Bit 15)
77	Logic Gnd	78	Logic Gnd
79		80	

1.6.8 BINARY/BCD 10^2 - 10^{-2} DECADES BOARD P/N 207730-2

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. No alignment or adjustment components are fitted to this board. For component location refer to figure 1-25.

Table 1-10 Binary/BCD 10^2 - 10^{-2} Decades Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 Vdc
B	10 (10^1 Decade Output)	2	80 (10^1 Decade Output)
C	Offset Binary Input (Bit 17)	3	40 (10^1 Decade Output)
D	200 (10^2 Decade Output)	4	20 (10^1 Decade Output)
E	Offset Binary Input (Bit 15)	5	0.8 (10^{-1} Decade Output)
F	Offset Binary Input (Bit 18)	6	0.4 (10^{-1} Decade Output)
H	100 (10^2 Decade Output)	7	0.2 (10^{-1} Decade Output)
J	0.1 (10^{-1} Decade Output)	8	0.08 (10^{-2} Decade Output)
K	0.002 10^3 Decade Output	9	0.04 (10^{-2} Decade Output)
L	0.001 10^{-3} Decade Output	10	0.02 (10^{-2} Decade Output)
M	0.004 10^{-3} Decade Output	11	0.01) (10^{-2} Decade Output)
N	0.008 10^{-3} Decade Output	12	Offset Binary Input (Bit 14)
P	Carry (Out)	13	2 (10^0 Decade Output)
R		14	4 (10^0 Decade Output)
S	8 (10^0 Decade Output)	15	Offset Binary Input (Bit 2)
T	Offset Binary Input (Bit 6)	16	Carry (IN)
U	1 (10^0 Decade Output)	17	Carry (IN)
V	10^{-3} Decade Carry (4)	18	10^{-3} Decade Carry (1)

Table 1-10 Binary/BCD 10^2 - 10^2 Decades Board, Pin Assignment (Continued)

Edge-pin	Input/Output	Edge-pin	Input/Output
W	Offset Binary Input (Bit 5)	19	10^{-3} Decade Carry (2)
X	Offset Binary Input (Bit 11)	20	Offset Binary Input (Bit 8)
Y	Offset Binary Input (Bit 9)	21	Offset Binary Input (Bit 4)
Z	Offset Binary Input (Bit 12)	22	Offset Binary Input (Bit 10)
AA	Offset Binary Input (Bit 16)	23	Offset Binary Input (Bit 14)
BB	Gnd	24	Gnd
CC		25	

1.6.9 BINARY/BCD 10^{-3} DECADE BOARD P/N 207733-3

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. No alignment or adjustment components are fitted. For component location refer to figure 1-26.

Table 1-11 Binary/BCD 10^{-3} Decade Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A	+5 Vdc	1	+5 Vdc
B	10^{-3} Decade Carry (1)	2	10^{-3} Decade Carry (2)
C	0.008 (10^{-3} Decade Output)	3	10^{-3} Decade Carry (4)
D	0.004 (10^{-3} Decade Output)	4	0.002 (10^{-3} Decade Output)
E		5	
F		6	
H	Gnd	7	Gnd
J		8	Gnd
K	0.001 (10^{-3} Decade Output)	9	
L	Offset Binary Input (Bit 4)	10	
M		11	Offset Binary Input (Bit 6)
N		12	
P		13	Offset Binary Input (Bit 11)
R		14	
S		15	Offset Binary Input (Bit 3)
T		16	Offset Binary Input (Bit 7)
U		17	
V		18	
W		19	Offset Binary Input (Bit 9)
X	Offset Binary Input (Bit 7)	20	Offset Binary Input (Bit 10)
Y		21	Offset Binary Input (Bit 12)
Z	Offset Binary Input (Bit 5)	22	Offset Binary Input (Bit 8)
AA	Offset Binary Input (Bit 8)	23	Offset Binary Input (Bit 2)
BB	Gnd	24	Gnd
CC	Offset Binary Input (Bit 13)	25	

1.6.10 DIFFERENTIAL LINE DRIVER BOARD P/N 212815-1

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) x 80 mm (3.12 in). Electrical connections are made through 80 edge-pins which form the lower edge of the board. Figure 1-27 indicates component location and the location of test point E1.

Table 1-12 Differential Line Driver Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
1	+5 Vdc	2	+5 Vdc
3	Data Output Bit 12 (LO)	4	Data Output Bit 13 (LO)
5	Data Output Bit 12 (HI)	6	Data Output Bit 13 (HI)
7	Data Output Bit 11 (HI)	8	Data Output Bit 14 (HI)
9	Data Output Bit 11 (LO)	10	Data Output Bit 14 (LO)
11	Data Input Bit 12	12	
13	Data Input Bit 11	14	Data Input Bit 18
15	Data Input Bit 13	16	Data Output Bit 15 (HI)
17	Data Input Bit 14	18	Data Output Bit 15 (LO)
19	Data Input Bit 15	20	Data Output Bit 18 (LO)
21	Data Input Bit 16	22	Data Output Bit 18 (HI)
23	Data Output Bit 16 (HI)	24	
25	Data Output Bit 16 (LO)	26	Data Output Bit 17 (LO)
27	Data Output Bit 5 (LO)	28	Data Output Bit 17 (HI)
29	Data Output Bit 5 (HI)	30	Data Input Bit 17
31	Data Output Bit 4 (LO)	32	Data Input Bit 4
33	Data Output Bit 4 (HI)	34	
35	Data Output Bit 3 (LO)	36	Data Output Bit 6 (HI)
37	Data Output Bit 3 (HI)	38	Data Output Bit 6 (LO)
39	Data Input Bit 6	40	Data Input Bit 3
41	Data Input Bit 5	42	
43	Data Output Bit 10 (LO)	44	Data Input Bit 10
45	Data Output Bit 10 (HI)	46	Data Input Bit 9
47	Data Output Bit 9 (HI)	48	
49		50	Data Output Bit 9 (LO)
51		52	Data Input Bit 7
53		54	Data Input Bit B
55	Data Output Bit B (HI)	56	
57	Data Output Bit A (HI)	58	Data Output Bit B (LO)
59	Data Output Bit A (LO)	60	Data Output Bit 7 (LO)
61	Data Input Bit A	62	Data Output Bit 7 (HI)
63	Data Output Bit C (LO)	64	Data Output Bit 8 (LO)
65	Data Output Bit C (HI)	66	Data Output Bit 8 (HI)
67	Data Input Bit 1	68	Data Input Bit 8
69	Data Input Bit 2	70	Data Input Bit C
71	Data Output Bit 2 (HI)	72	Data Input Bit D
73	Data Output Bit 2 (LO)	74	Data Output Bit D (LO)
75	Data Output Bit 1 (HI)	76	Data Output Bit D (HI)
77	Gnd	78	Gnd
79	Data Output Bit 1 (20)	80	

1.6.11 1200 Hz OSCILLATOR BOARD P/N 211190-5

This LRU is a rigid pcb measuring approximately 130 mm (5.07 in) X 80 mm (3.12 in). Electrical connections are made through 50 edge-pins which form the lower edge of the board. Figure 1-28 indicates component location and the location of the two SAT resistors R3 and R11.

Table 1-13 1200 Hz Oscillator Board, Pin Assignment

Edge-pin	Input/Output	Edge-pin	Input/Output
A		1	
B	-15 Vdc	2	-15 Vdc
C	+15 Vdc	3	+15 Vdc
D		4	
E	Test Point	5	Test Point
F		6	
H		7	
J	3.7 V output	8	3.7 V output
K		9	
L		10	
M		11	
N		12	
P		13	
R		14	
S		15	
T		16	
U		17	
V		18	
W		19	
X	1200 Hz, 12 V Output (Hl)	20	1200 Hz, 12 V Output (HI)
Y	1200 Hz, 12 V Output (LO)	21	1200 Hz, 12 V Output (LO)
Z		22	
AA		23	
BB	Sig Gnd	24	Sig Gnd
CC		25	

1.6.12 EXTENDER BOARD, 80-way P/N 212189-1

This LRU is a rigid double-sided pcb measuring approximately 130 mm (5.07 in) x 100 mm (3.9 in) which carries 80 straight-through tracks. Electrical connections are made through an 80-way edge-connector secured to the upper edge of the board and 80 edge-pins which form the lower edge of the board. Refer to figure 1-29.

1.6.13 EXTENDER BOARD, P/N 211300-1

This LRU is a rigid double-sided pcb measuring approximately 130 mm (5.07 in) x 100 mm (3.9 in) which carries 50 straight-through tracks. Electrical connections are made through a 50-way edge-connector secured to the upper edge of the board and 50 edge-pins which form the lower edge of the board. Refer to figure 1-30.

1.6.14 15 VDC POWER SUPPLY-R115

This LRU is of rectangular construction in an enclosed case measuring 437 mm (1.72 in) x 187 mm (7.36 in) x 89 mm (3.5 in) and weighting 2.025 kg (4.5 lbs). The unit contains chassis mounted components and a printed circuit board. Component location for the printed circuit board is shown on figure 1-31.

1.6.15 5 VDC POWER SUPPLY ASSEMBLY-210

This LRU is of rectangular construction in an enclosed case measuring 128.6 mm (5.06 in) x 101.6 mm (4.0 in) x 57.2 mm (2.25 in) and weighing 0.9 kg (2.0 lbs). The unit contains chassis mounted components and a printed circuit board. Component location for the printed circuit board is shown on figure 1-32.

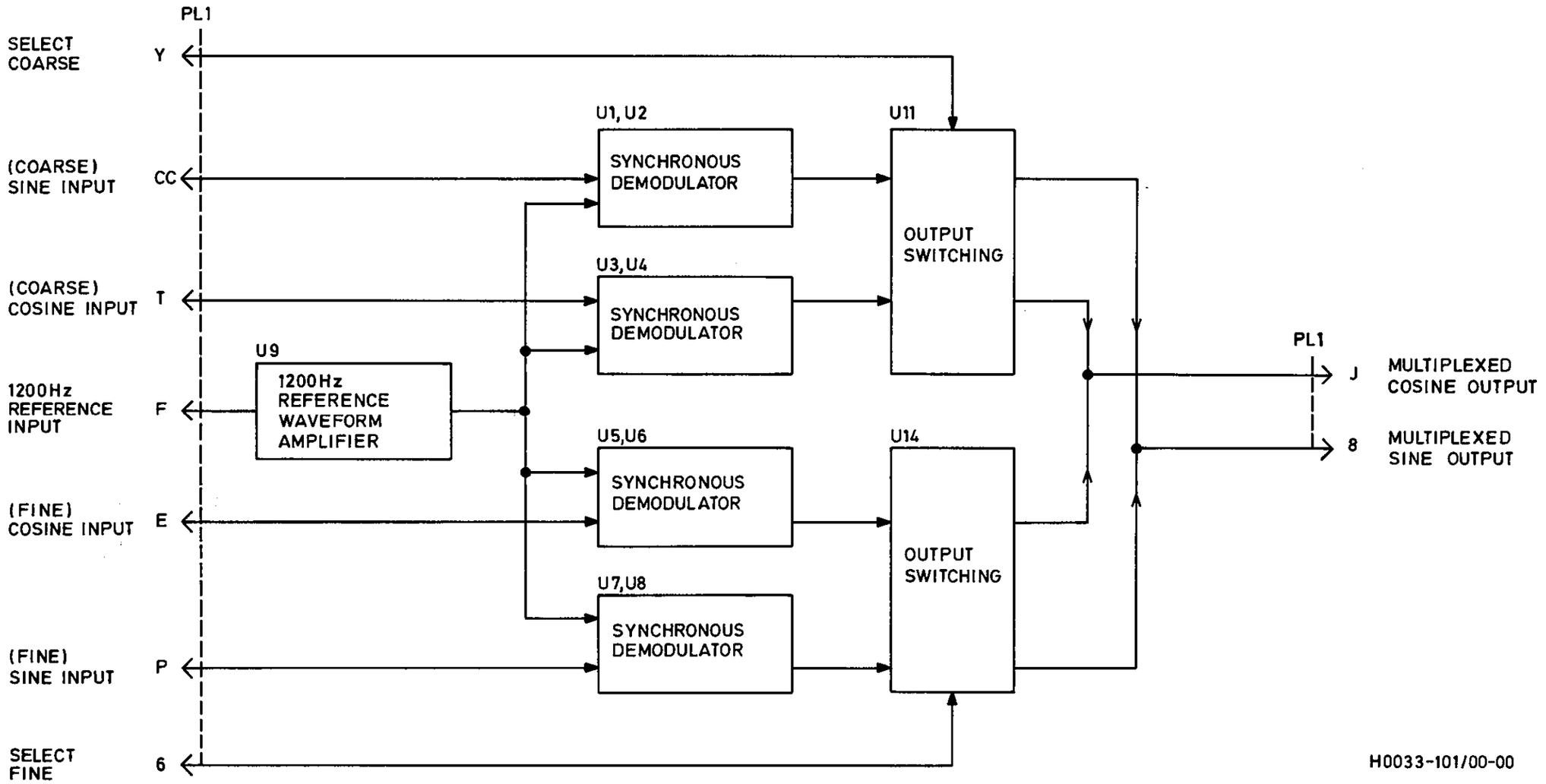
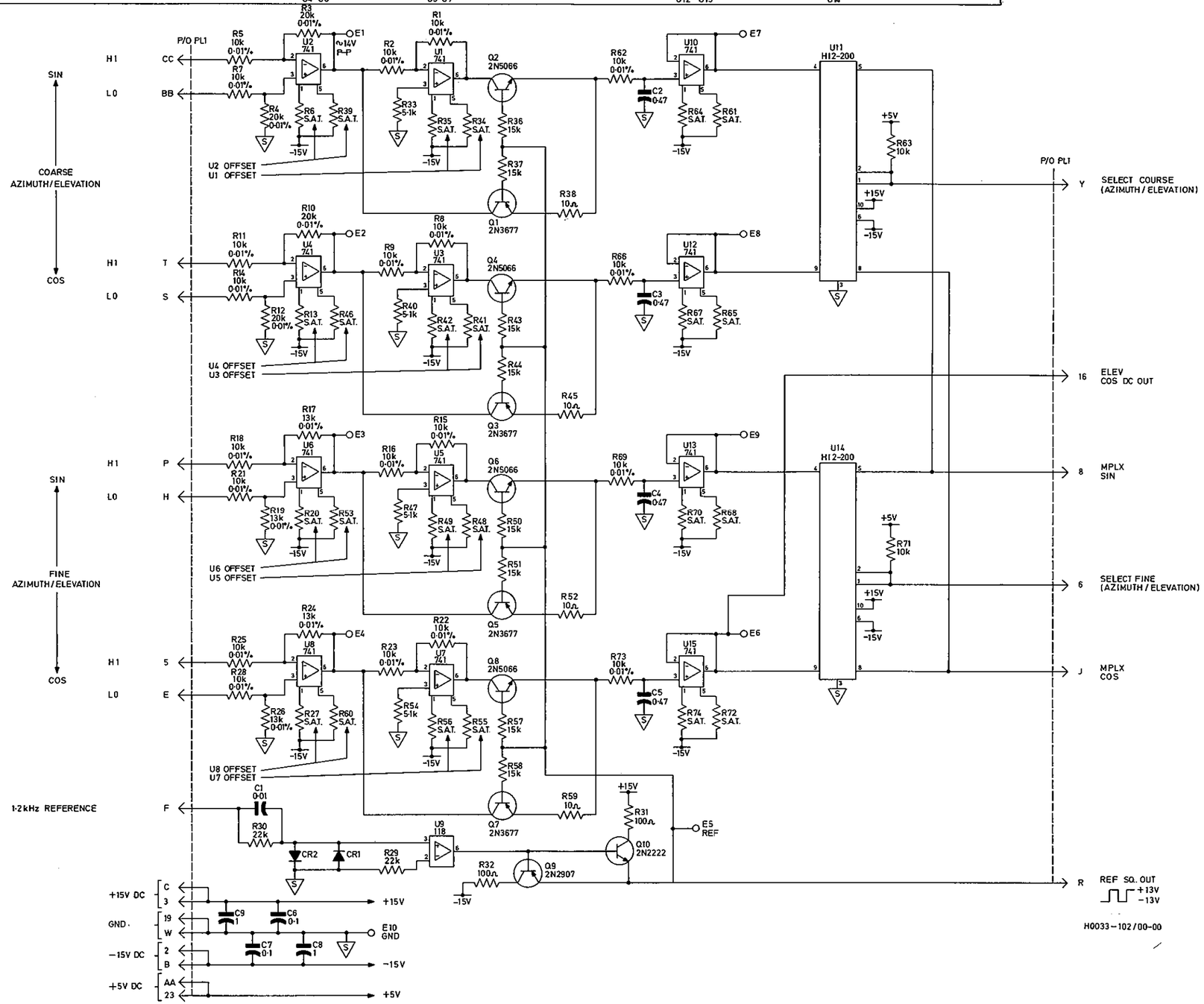


Figure 1-1. Synchronous Demodulator/Multiplexer Board, Functional Block Diagram

RESISTORS	R5 R11 R18 R25 R4 R19 R7 R14 R21 R28 R12 R26 R30 R6 R20 R3 R17 R39 R53 R2 R16 R13 R27 R10 R24 R46 R60 R9 R23 R29 R33 R47 R35 R49 R1 R15 R34 R48 R40 R54 R42 R56 R8 R22 R41 R55 R32 R36 R43 R50 R57 R38 R52 R62 R69 R31 R37 R44 R51 R58 R45 R59 R66 R73 R64 R70 R61 R68 R67 R74 R65 R72 R63 R71
CAPACITORS	C9 C7 C1 C6 C8 C2 C5
MISCELLANEOUS	CR2 U2 U6 U4 U8 CR1 U1 U5 U3 U7 U9 Q1---Q9 Q10 U10 U13 U12 U15 U11 U14



NOTES:
1. ALL RESISTORS ARE 1/8W, 0·01% ARE MPC'S.
2. ALL DIODES ARE 1N4148.
3. ON IC'S U1–10,12,13,15 PIN 7 IS +15V AND PIN 4 IS −15V
4. C2,C3,C4 AND C5 ARE MATCHED TO 0·1%.

Figure 1-2. Synchronous Demodulator/Multiplexer Board, Schematic Diagram

P/N 212195-6

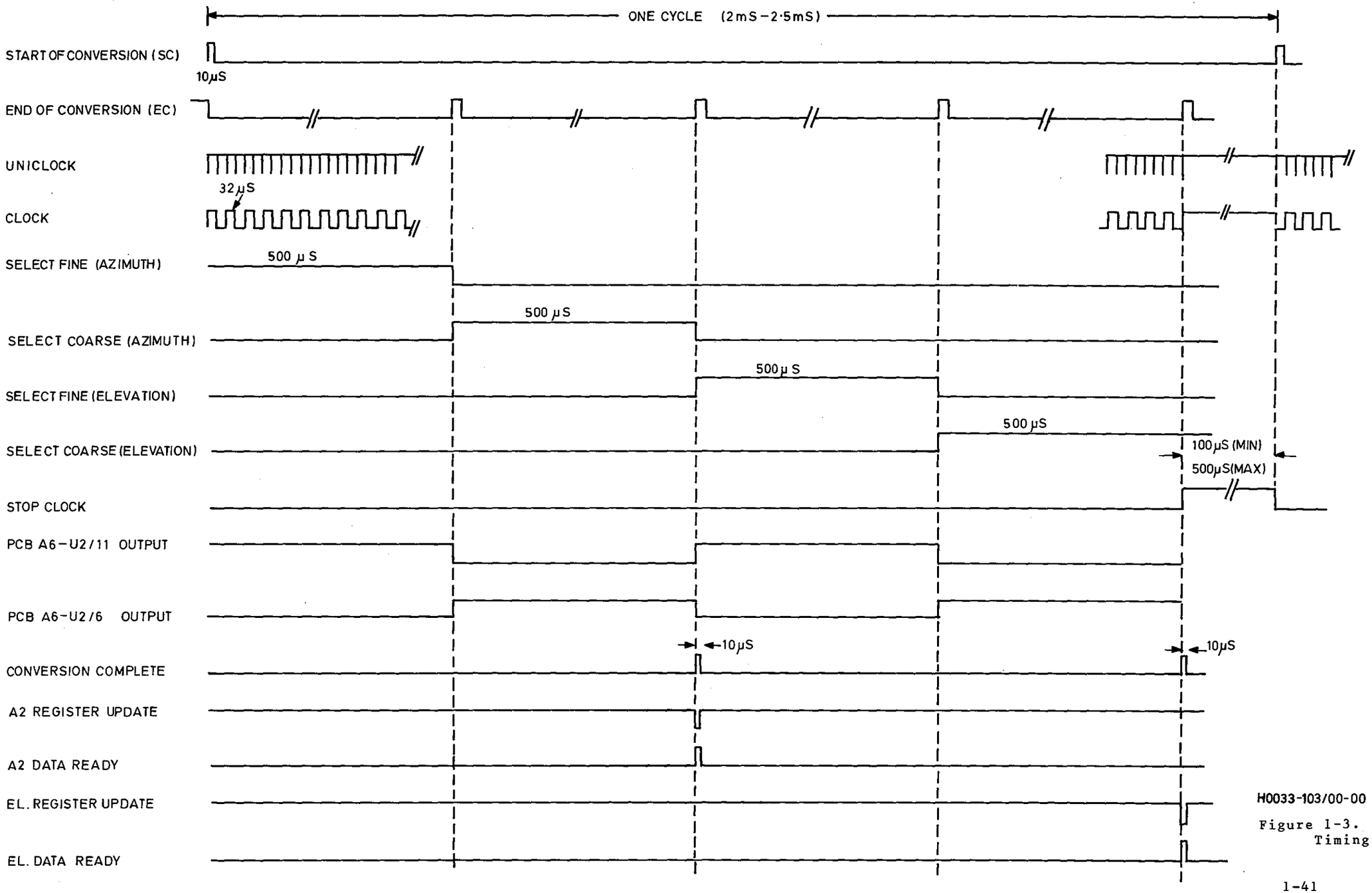


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Figure 1-3. Overall Timing Diagram

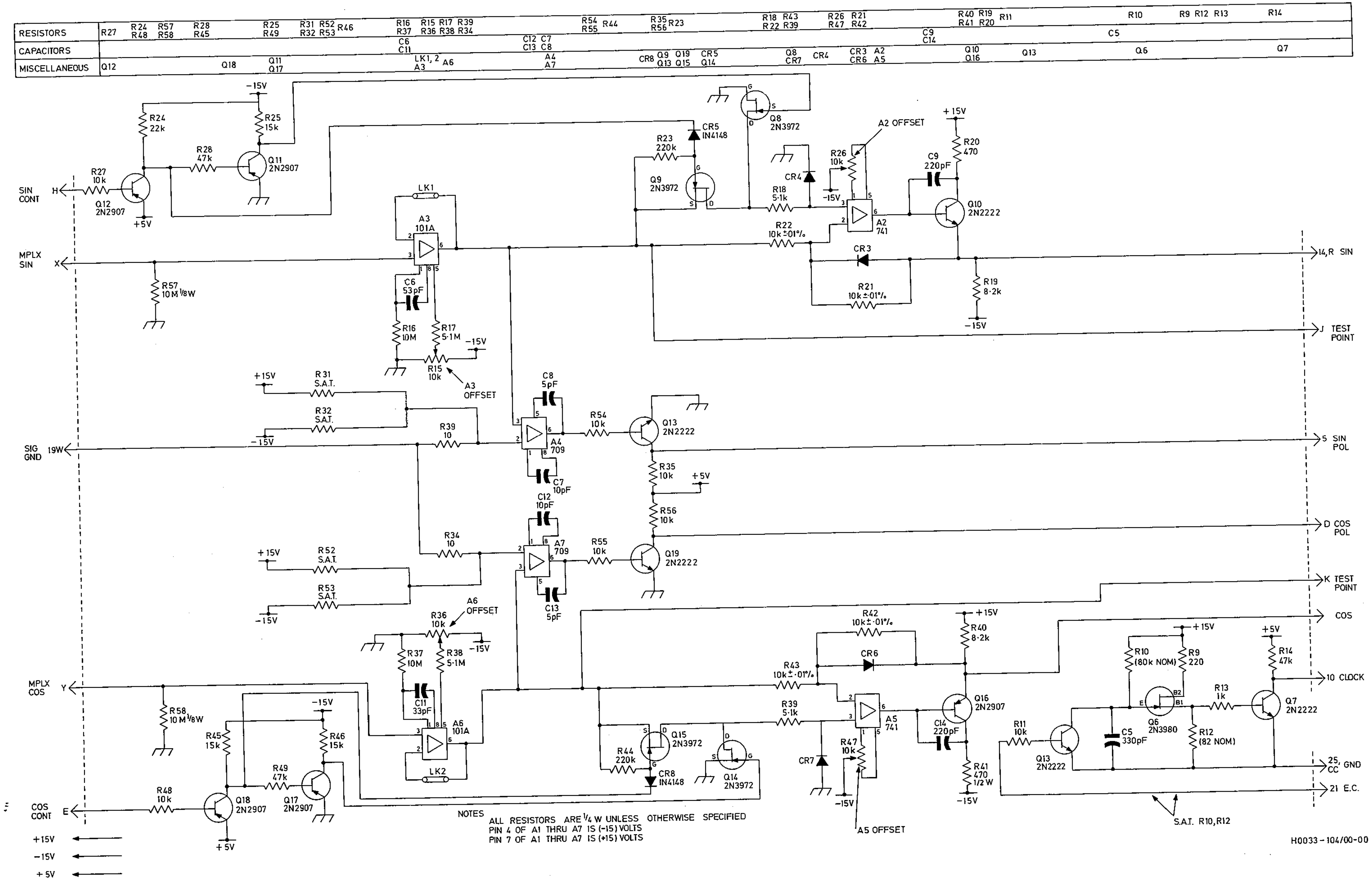

Figure 1-4. Signal Conditioning Board, Schematic Diagram

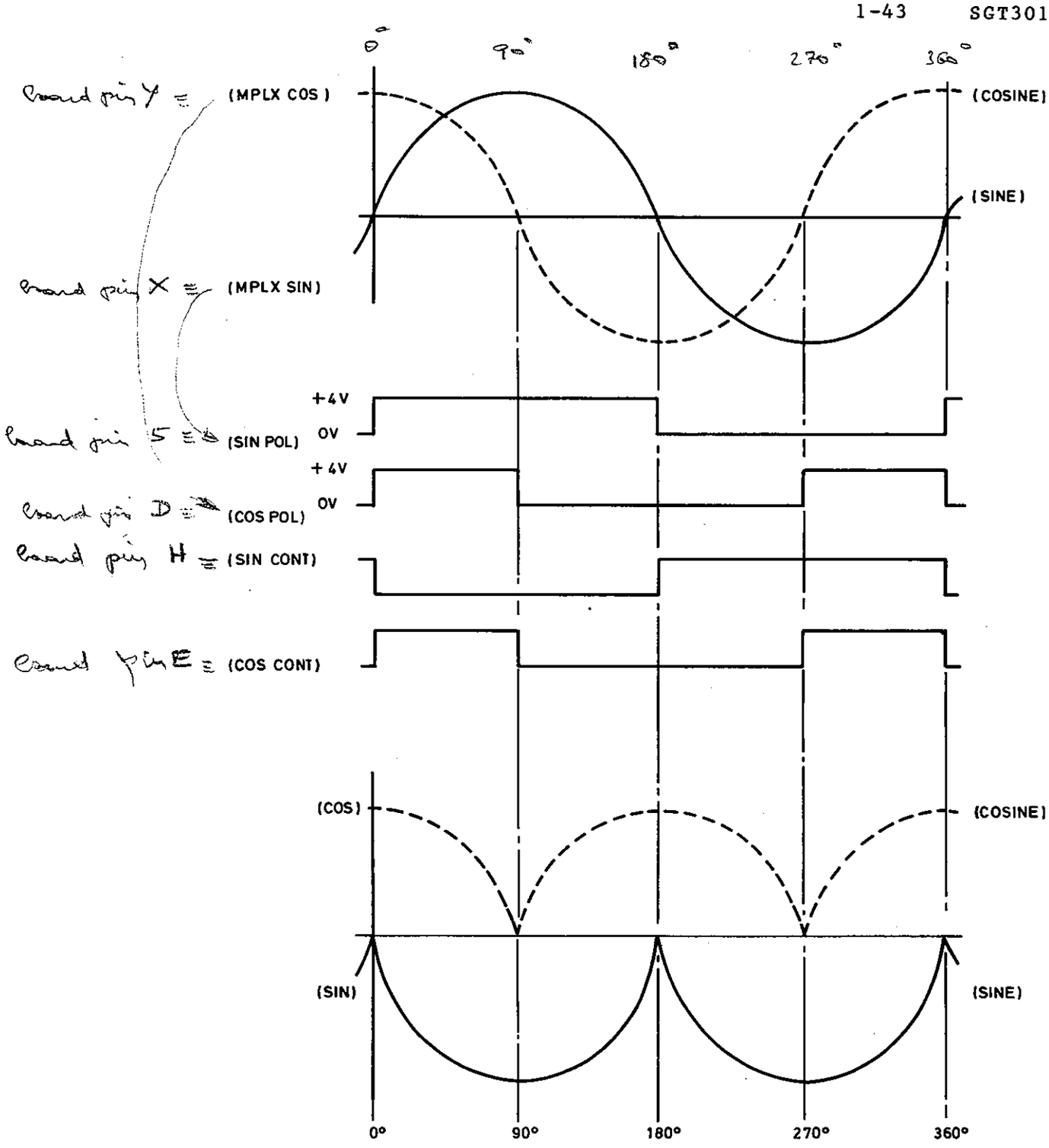

Figure 1-5. Signal Conditioning Board, Sine-Cosine Signals, Phase Relationship

RESISTORS	R85 R48 R78 R77 R45 R44 R69 R68 R30 R22 R21 R60 R59 R40 R16 R41 R49 R87 R88 R102 R89 R36 R110 R111 R93 R94 R15 R10 R9 R119 R120 R1 R128 R129 R31 R33 R97 R32 R98 R99 R100 R34 R101 R137 R135
CAPACITORS	C3 C1 C2
MISCELLANEOUS	Q36 Q24 Q35 Q23 Q34 Q22 Q33 Q21 Q32 Q20 Q31 Q19 Q10 Q30 Q18 Q9 Q29 Q17 Q8 Q28 Q16 Q7 Q27 Q15 Q6 Q26 Q14 Q25 Q13,12 CR1 Q37,38 Q50 CR2 Q51 Q39 Q5 Q52 Q40 Q4 Q53 Q41 Q3 Q54 Q42 Q2 Q55 Q43 Q1 Q56 Q44 Q57 Q45 Q58 Q46 Q59 Q47 A1709 Q60 Q48 Q61 Q49 Q11

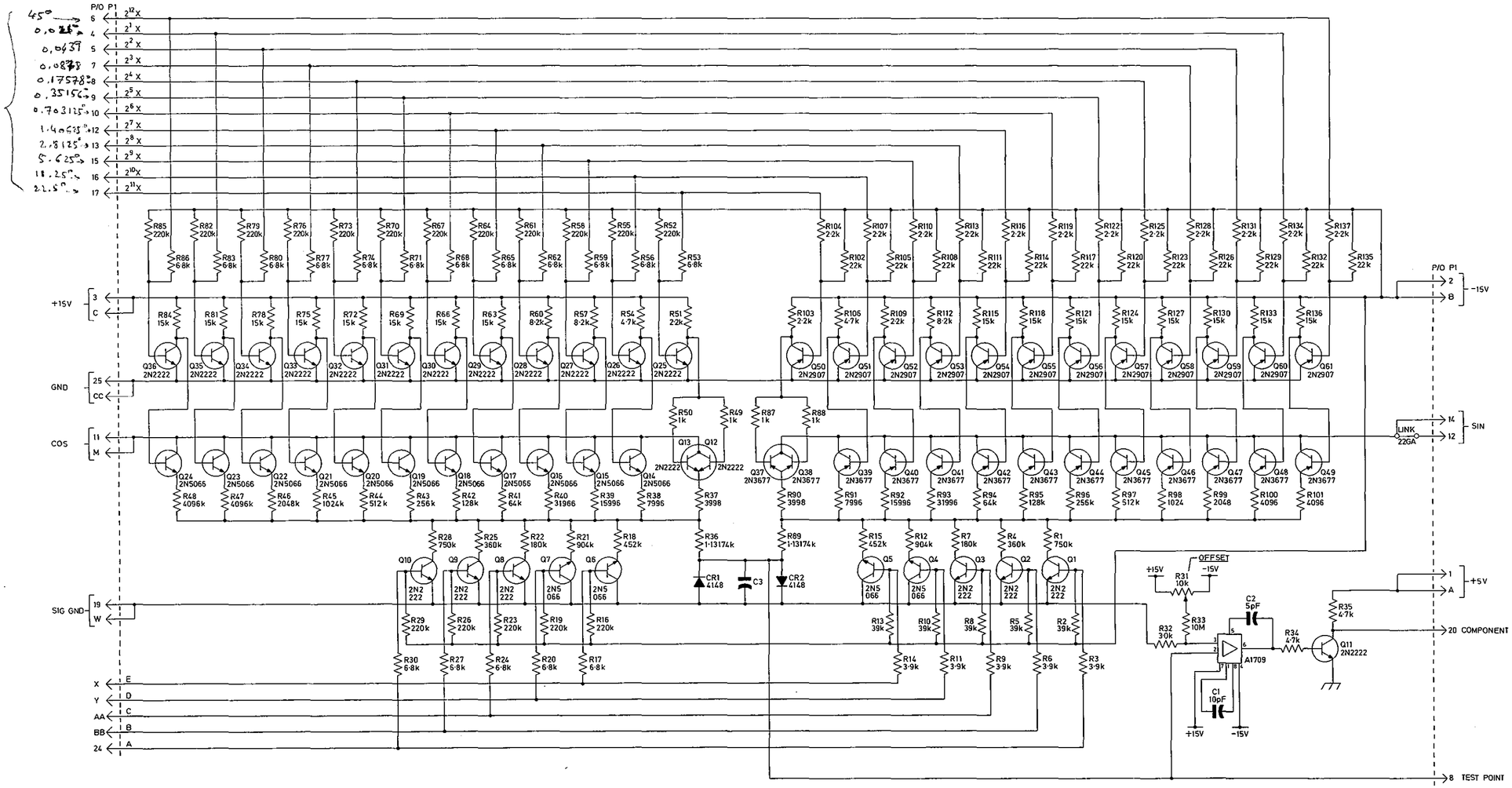

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Figure 1-6. Sin/Cos Network Board, Schematic Diagram

RESISTORS	R7 R8 R3 R5 R4 R9 R6 R2 R10 R11 R12 R1
CAPACITORS	C4 C1 C3 C2 C5 C6 C7
MISCELLANEOUS	U11a,b U15d U6a U10 U16b U15a U4c U17e U16d U17f U6b U17d U10a U2a U15f U1a U1c U16c U10c U1f U17c U1e U2b U17a U1b U16a U1d U15a U15c U4b U15b U4a U13f U3f U13e U5 U3a U13d U4f U13b U3b U13a U4e U13c U3e U4d U9a,b,c,d U7a,b,c,d U12 b,c,d U14 a,b,c,d U8f U17b

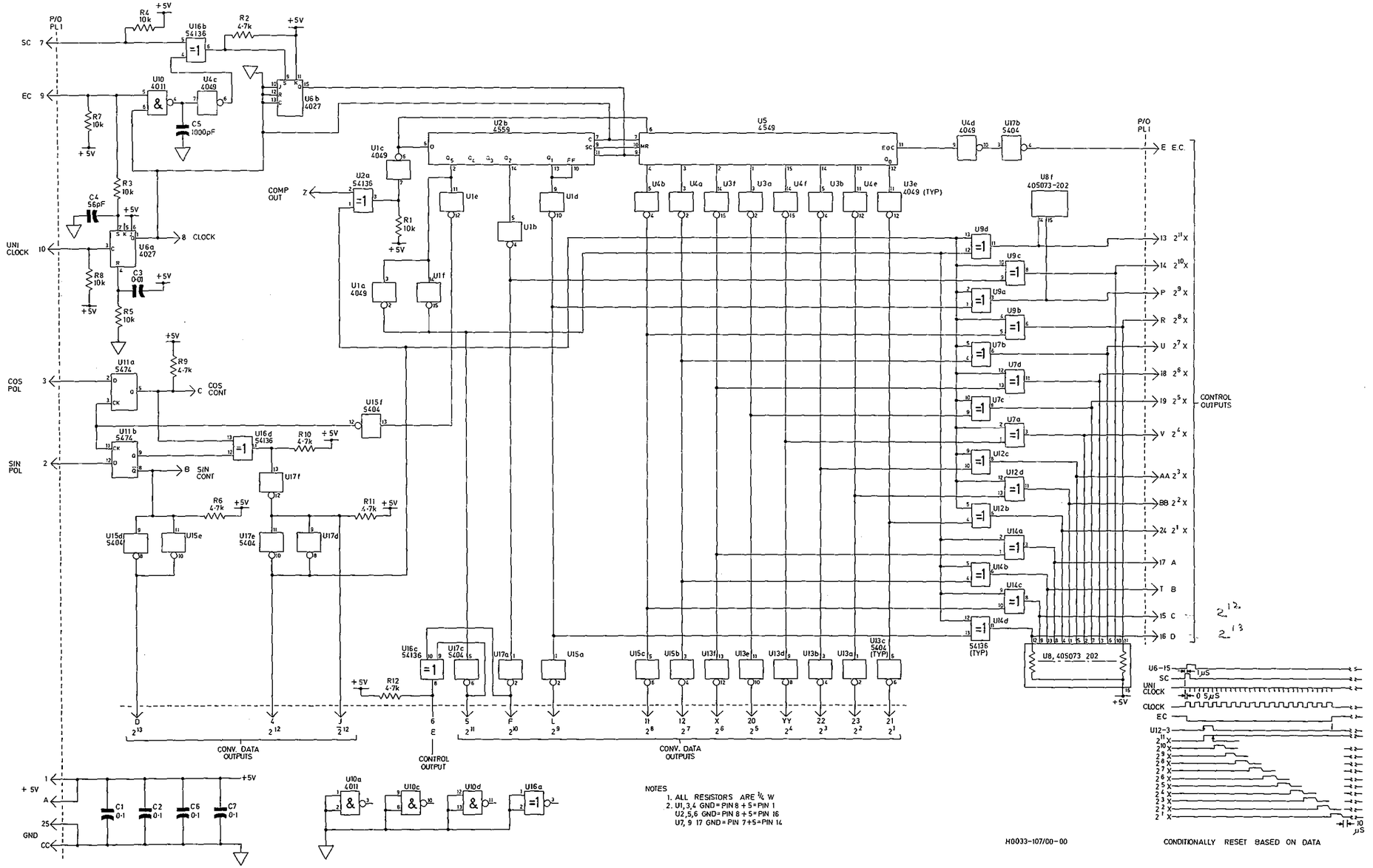
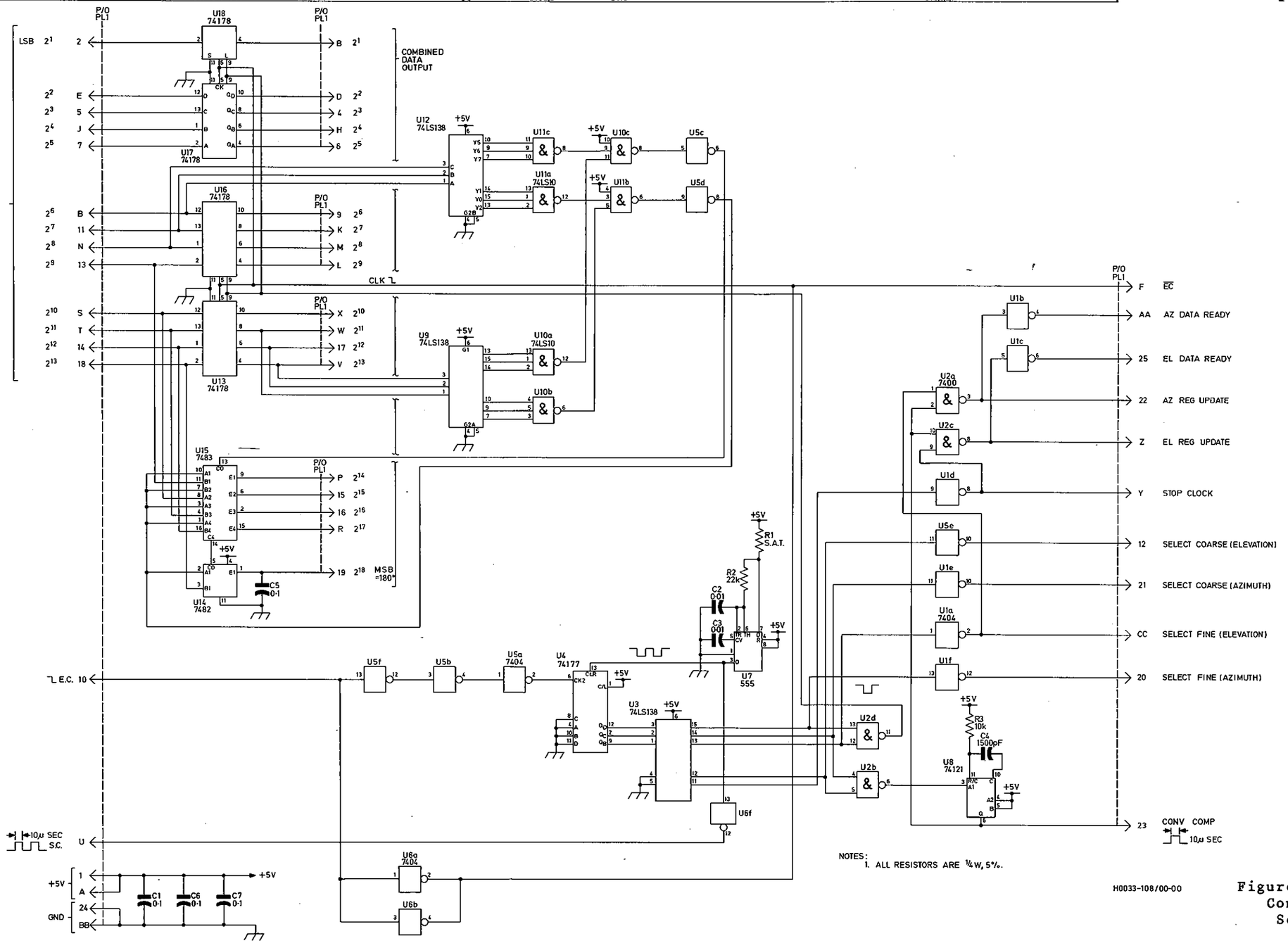


Figure 1-7. Successive Approximation Board, Schematic Diagram

RESISTORS	R2 R1 R3
CAPACITORS	C1 C6 C7 C5 C2 C3 C4
MISCELLANEOUS	U18 U16 U15 U17 U13 U14 U5f U6a,b U5b U12 U9 U5a U11c,a U10a,b U4 U10c U11b U3 U5c,d U6f U7 U2d,b U2a,c U1d,e,a,f U5e U8 U1b,c



NOTES:
1. ALL RESISTORS ARE ¼W, 5%.

H0033-108/00-00

Figure 1-8. Address/ Combination Board, Schematic Diagram

RESISTORS	R1 R3 R2 R4
CAPACITORS	C1 C2
MISCELLANEOUS	U3 U9 U6 U1 U7 U5 U4 U2 U8

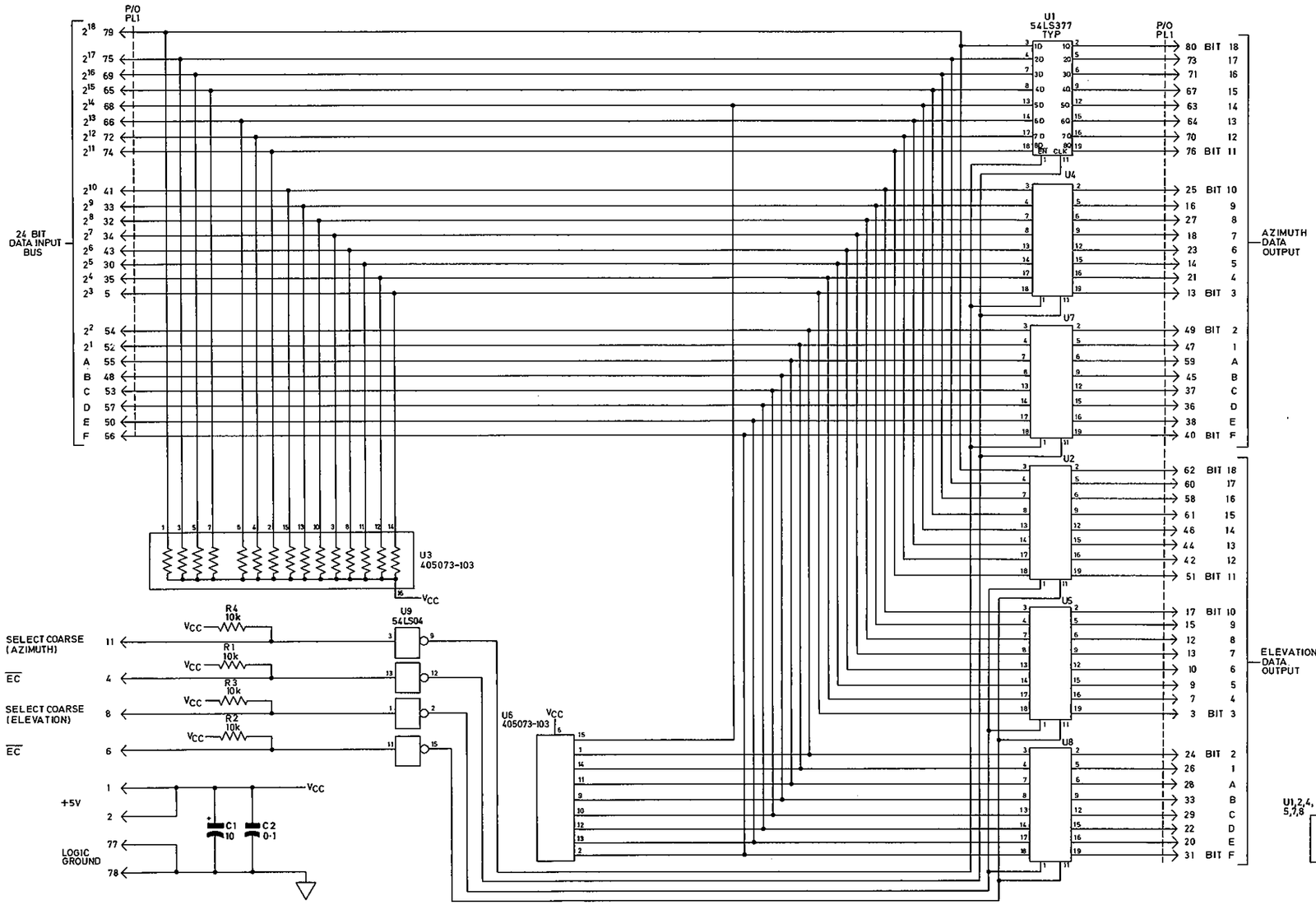


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Figure 1-9. Dual Output Registers Board, Schematic Diagram

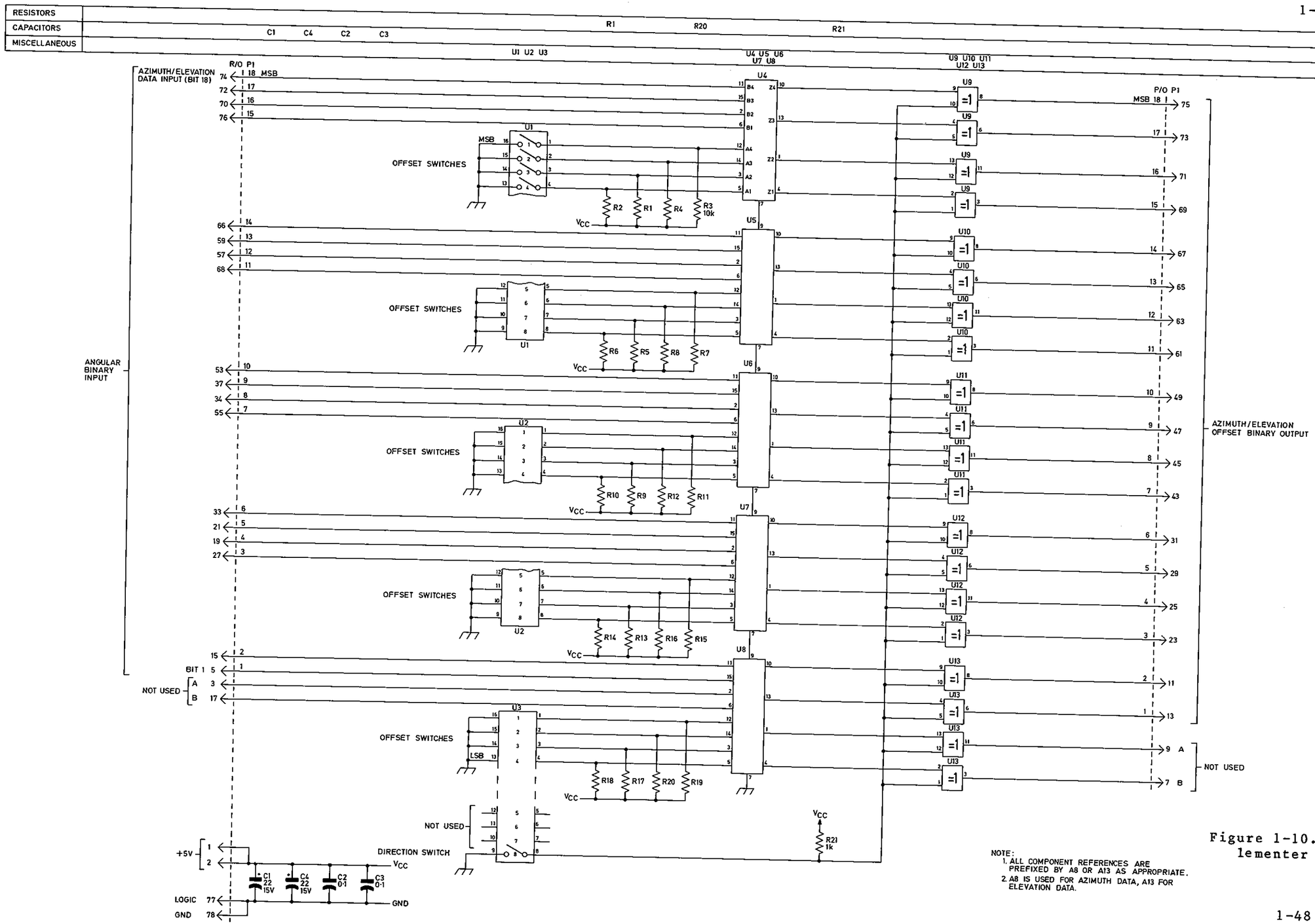

Figure 1-10. Adder/Complementer Board, Schematic Diagram

NOTE:
1. ALL COMPONENT REFERENCES ARE PREFIXED BY A8 OR A13 AS APPROPRIATE.
2. A8 IS USED FOR AZIMUTH DATA, A13 FOR ELEVATION DATA.

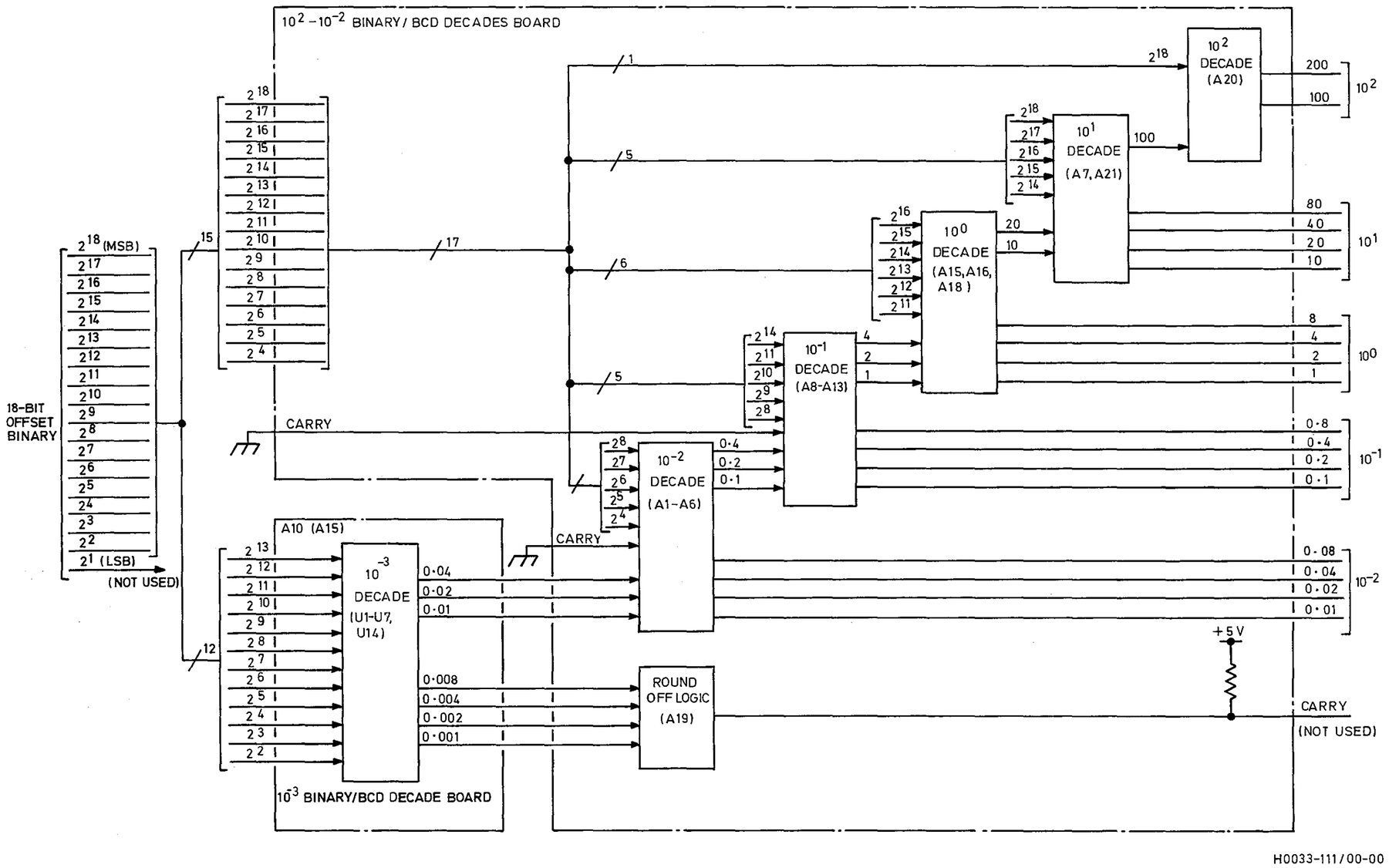

Figure 1-11. Binary/BCD Conversion, Functional Block Diagram

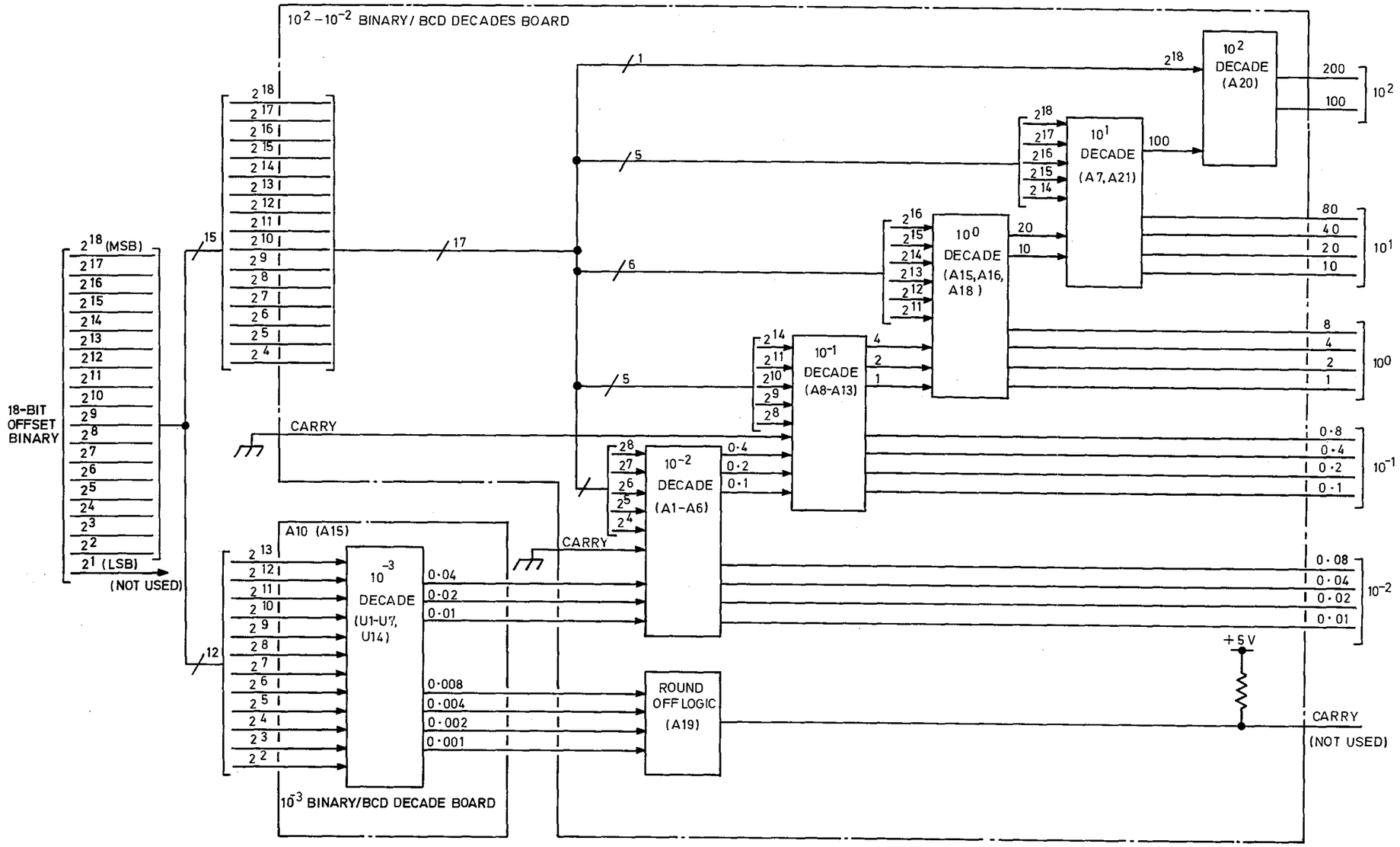

Figure 1-11. Binary/BCD Conversion, Functional Block Diagram

RESISTORS	R1 R3
CAPACITORS	
MISCELLANEOUS	U14 U1-U7

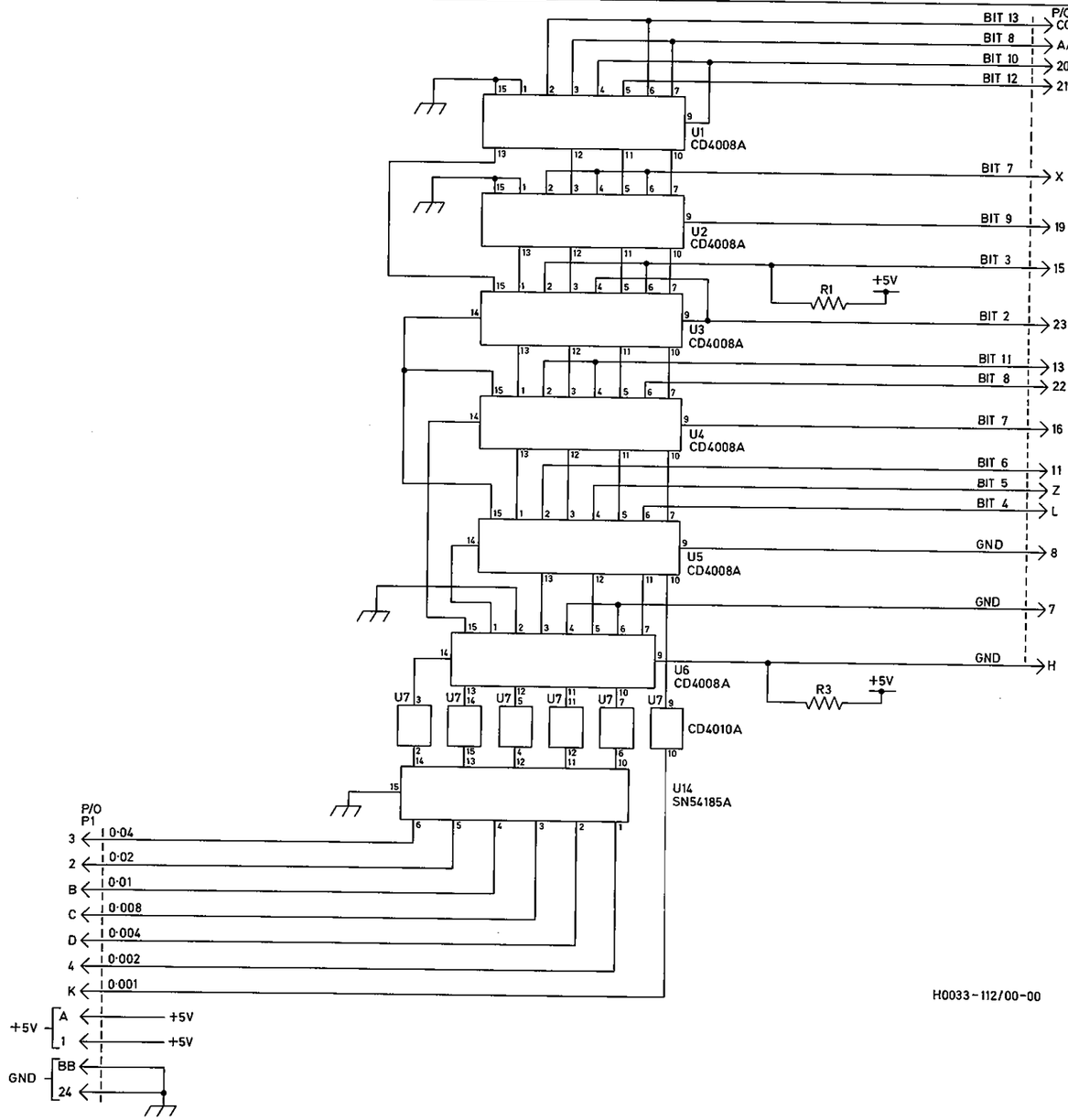

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Figure 1-12. Binary/BCD 10^{-3} Decade Board, Schematic Diagram

RESISTORS	R18 R8 R19 R7 R10 R25 R9 R23 R15 R16 R14 R26 R22 R24 R27 R2 R11 R3 R21 R4 R20 R1 R13 R5 R6 R12 R17
CAPACITORS	
MISCELLANEOUS	A19 A20 A21 A14 A7 A18 A17 A16 A13 A12 A13 A11 A10 A9 A8 A4 A5 A6 A3 A2 A1

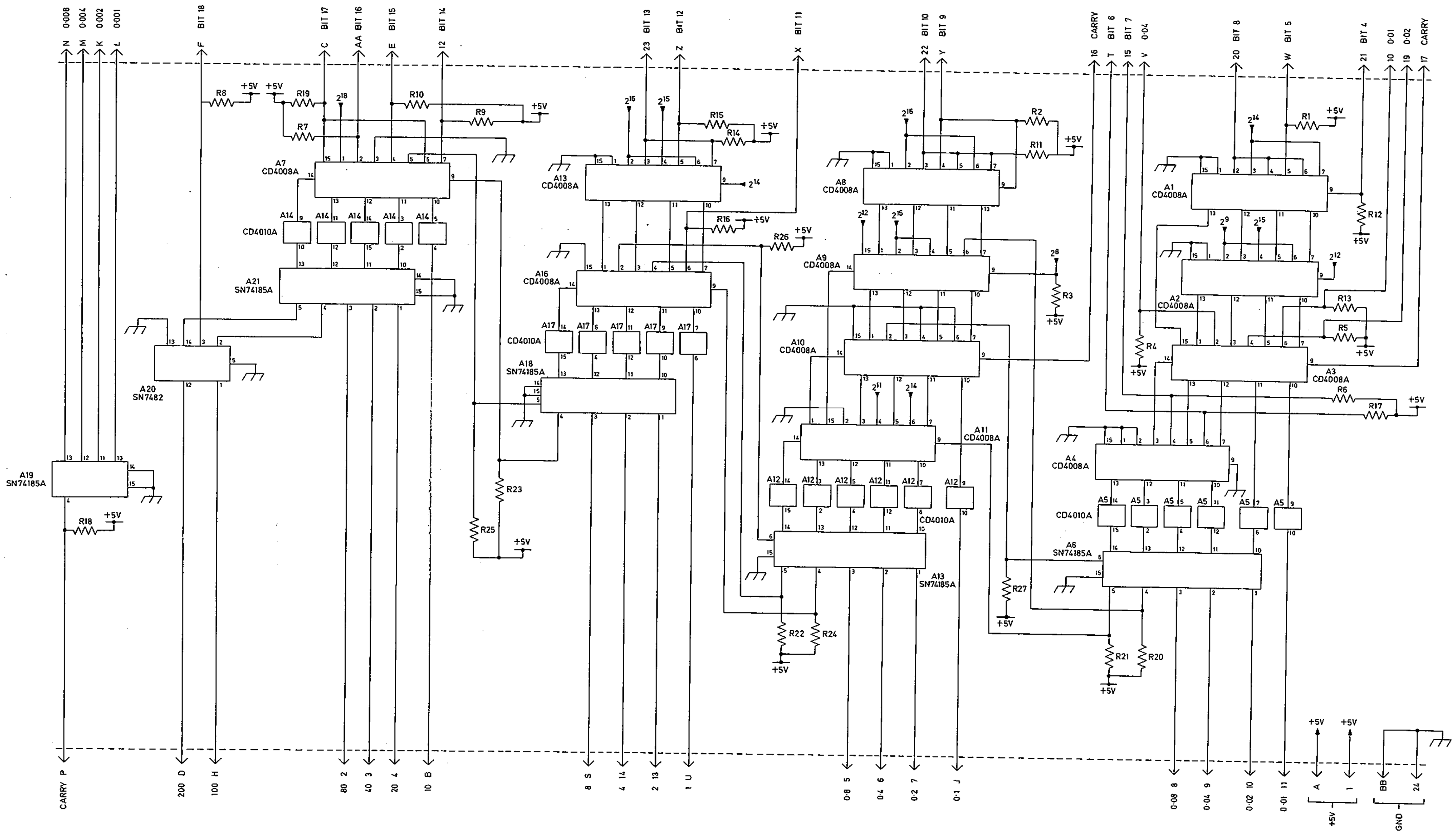

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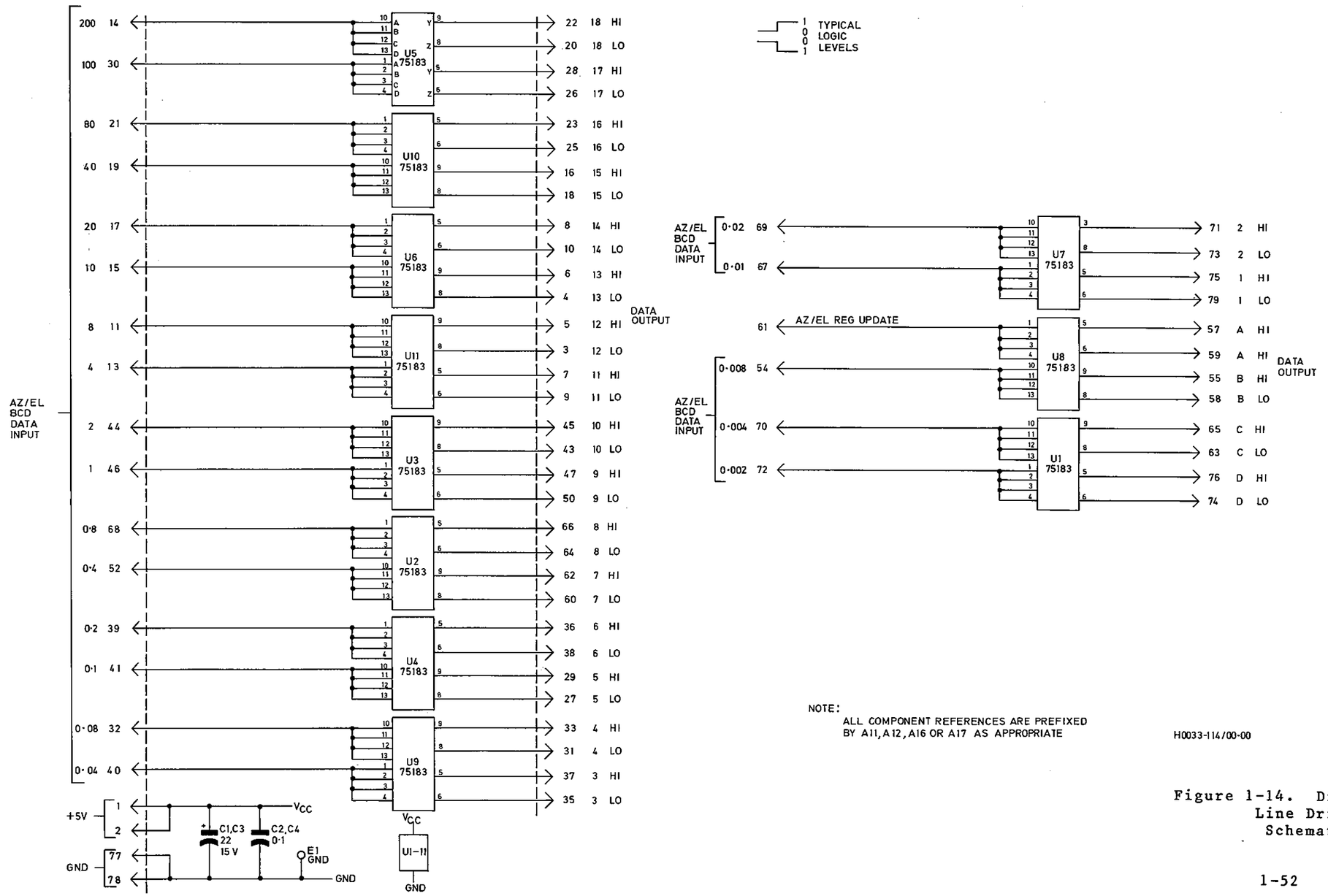
Figure 1-13. Binary/BCD 10^2 to 10^{-2} Decades Board Schematic Diagram

CAPACITORS	C1 C2 C3 C4
RESISTORS	
MISCELLANEOUS	U5 U6 U3 U4 U10 U11 U2 U9 U7 U8 U1



NOTE:
ALL COMPONENT REFERENCES ARE PREFIXED BY A11, A12, A16 OR A17 AS APPROPRIATE

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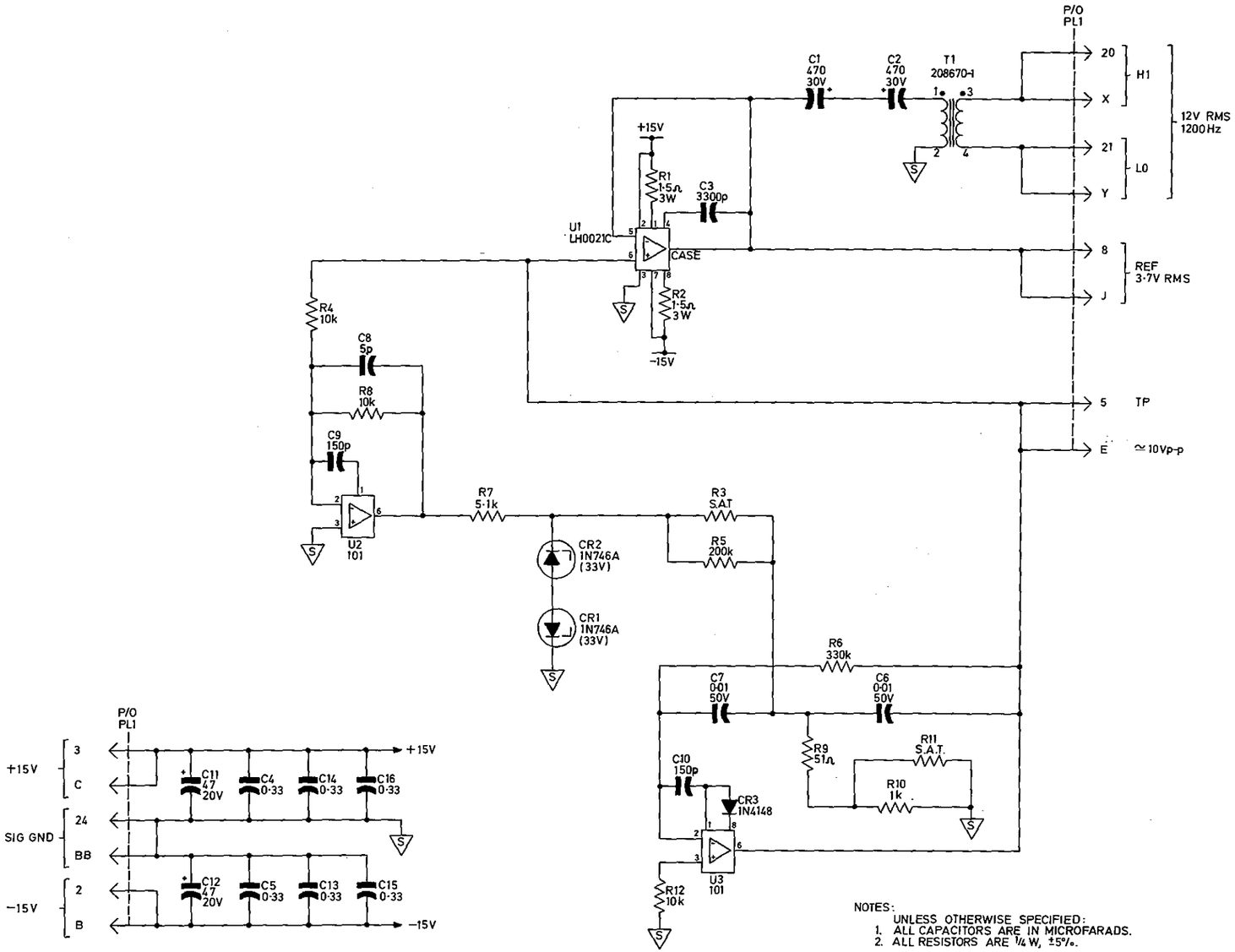
Figure 1-14. Differential Line Driver Board, Schematic Diagram

RESISTORS	R4 R8 R7 R1 R2 R12 R3 R5 R9 R6 R10 R11
CAPACITORS	C11 C12 C4 C5 C14 C13 C9 C8 C16 C15 C10 C3 C7 C1 C6 C2
MISCELLANEOUS	U2 CR2 CR1 U1 U3 CR3 T1



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE ¼ W, ±5%.

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Figure 1-15. 1200 Hz Oscillator Board, Schematic Diagram

RESISTORS	R1 R16, R2 R17, R3, R19 R18, R4 R5, R6, R7 R21, R8, R26, R10, R27, P1 R20, R9, R11, R28 R29, R30, R22, R12 R25, R13, R14 R23, R15 P2, R24, R31
CAPACITORS	C1, C5 C2, C6, C3, C4, C10, C7, C9, C8
MISCELLANEOUS	S1, T1, D3 D4, D1 D2, Q2, Q1, A1, Q3, Q6, Q7, Z1 Z2, Q4 Q5, Q8, A2, D7, D6, SI-1

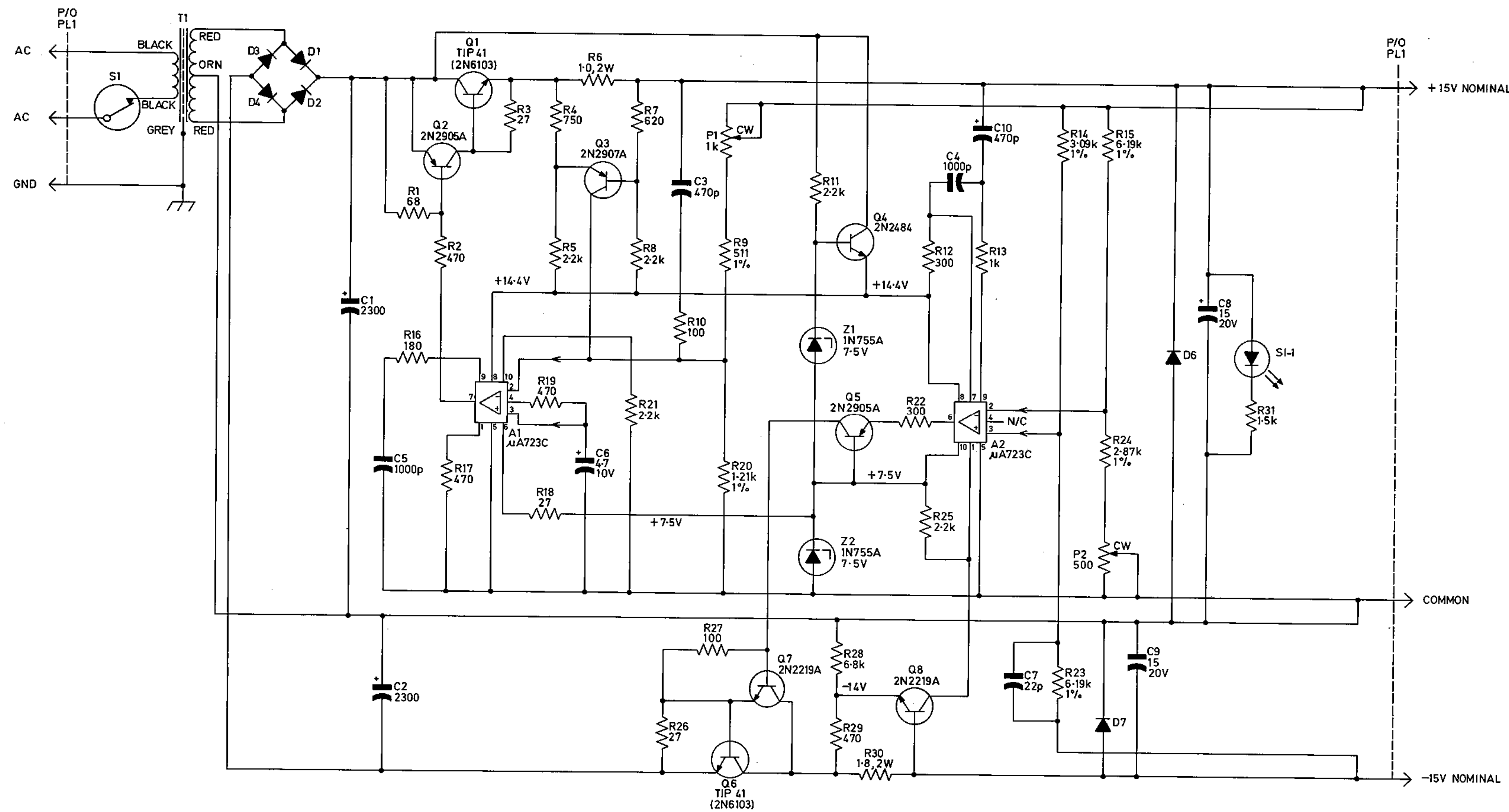
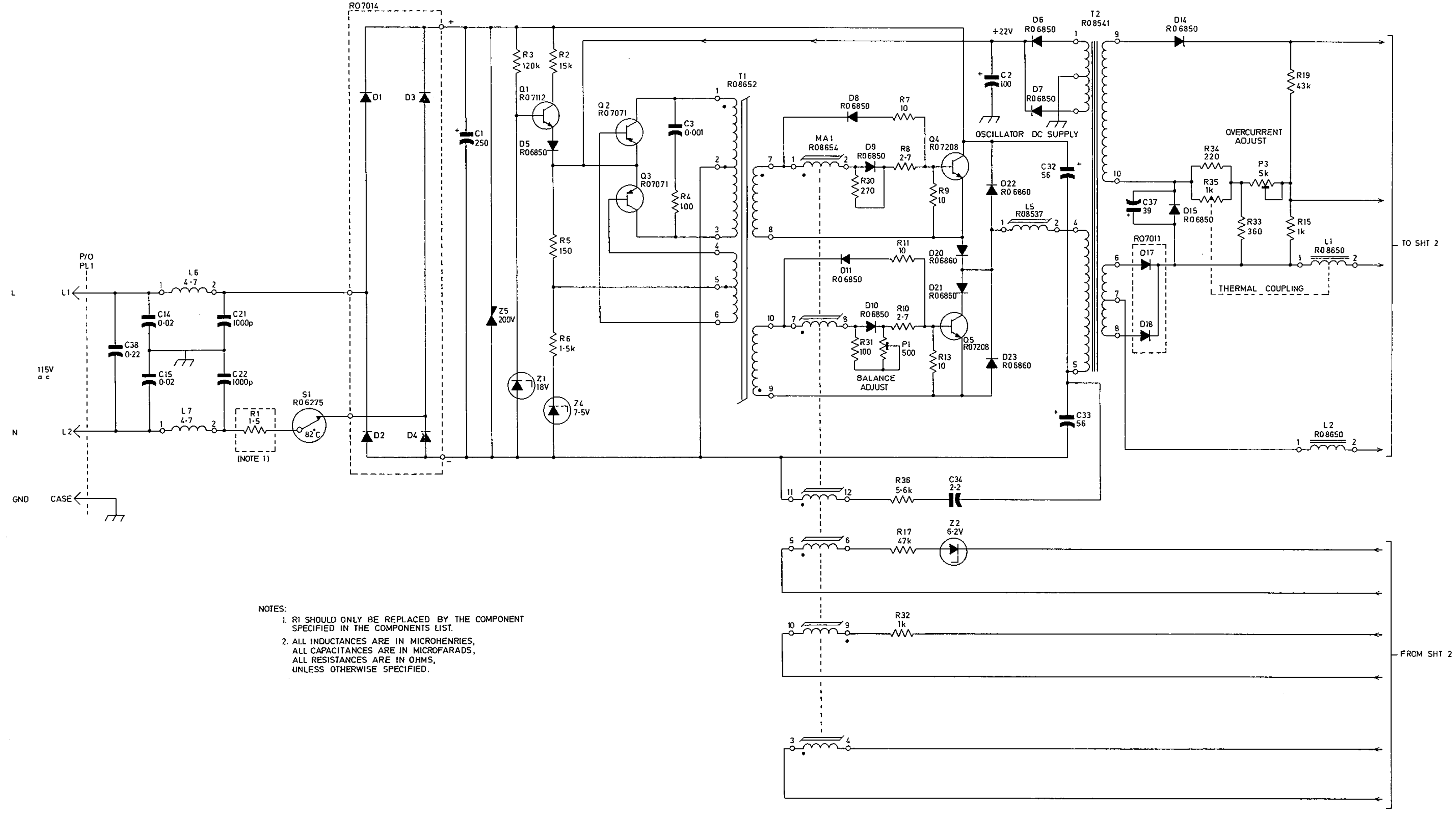


Figure 1-16. ± 15 Vdc Power Supply Assembly-R115, Schematic Diagram

RESISTORS	R1 R3 R2 R5 R6 R4 R30 R31 R7 R8 R11 R10 R36 R17 R32 R9 R13 R34 R35 R33 R19 R15
CAPACITORS	C38 C14 C15 C21 C22 C1 C3 C34 C2 C32 C33 C37
MISCELLANEOUS	L6 S1 D1 D2 D3 D4 Z5 Q1 D5 Z1 Z4 Q2 Q3 T1 MA1 D11 D8 D9 D10 P1 Q4 D20 D21 Q5 Z2 D22 D23 L5 D7 D6 T2 D17 D18 D15 P3 L1 L2



NOTES:
1. R1 SHOULD ONLY BE REPLACED BY THE COMPONENT SPECIFIED IN THE COMPONENTS LIST.
2. ALL INDUCTANCES ARE IN MICROHENRIES, ALL CAPACITANCES ARE IN MICROFARADS, ALL RESISTANCES ARE IN OHMS, UNLESS OTHERWISE SPECIFIED.

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Figure 1-17. +5 Vdc Power Supply Assembly 210, Schematic Diagram (Sheet 1)

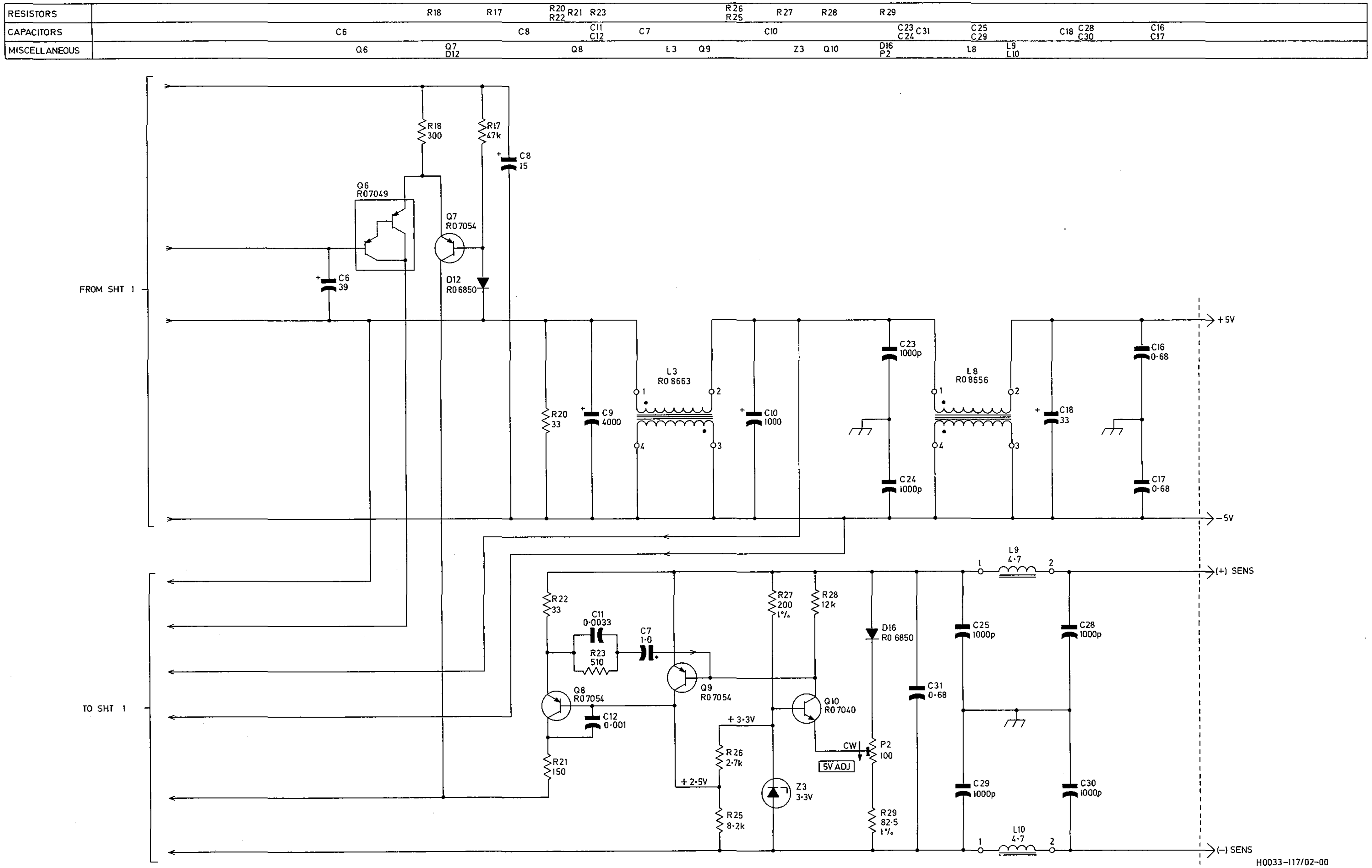

Figure 1-17. +5 Vdc Power Supply Assembly 210, Schematic Diagram (Sheet 2)

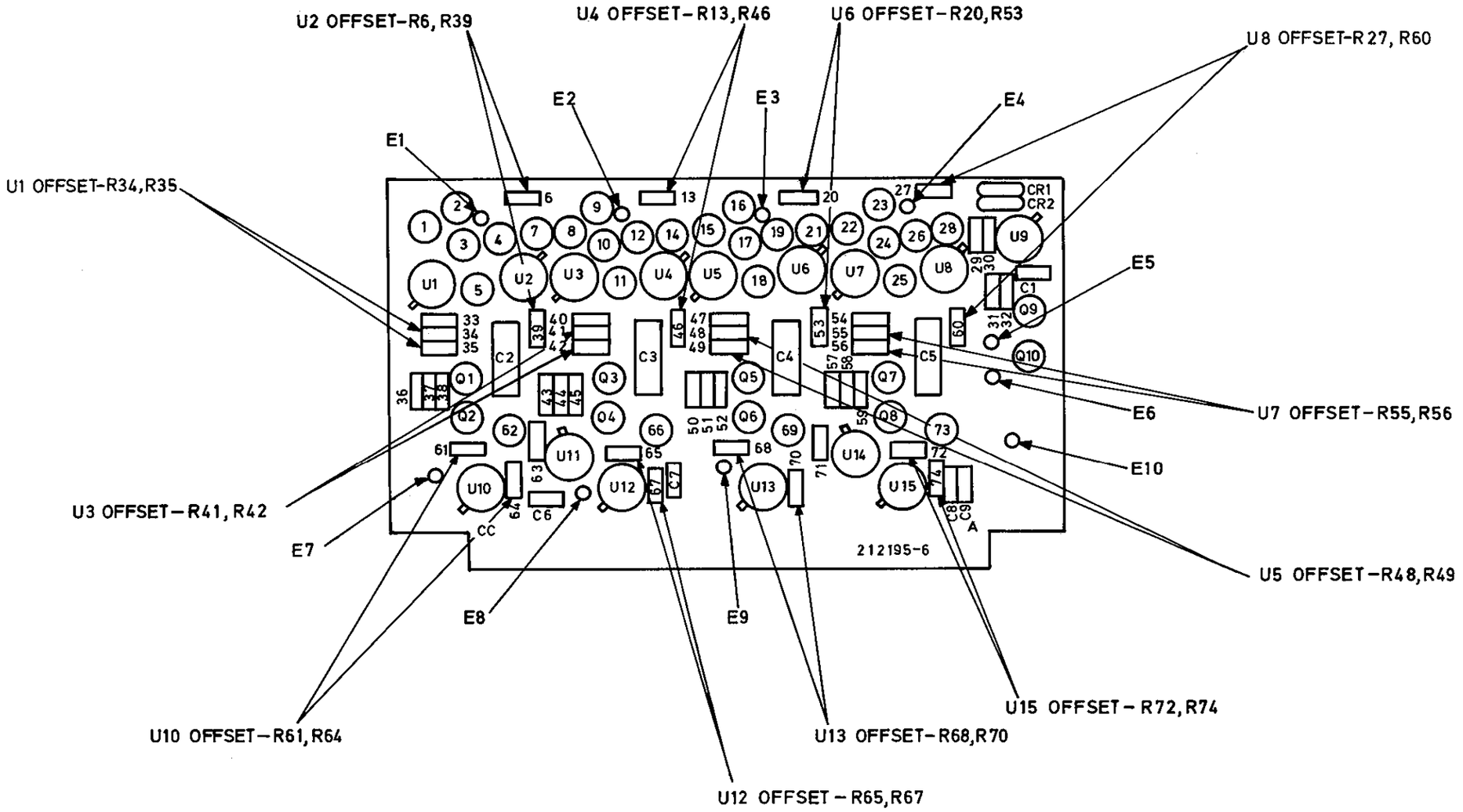

Figure 1-18. Synchronous Demodulator/Multiplexer Board, Component Location Diagram

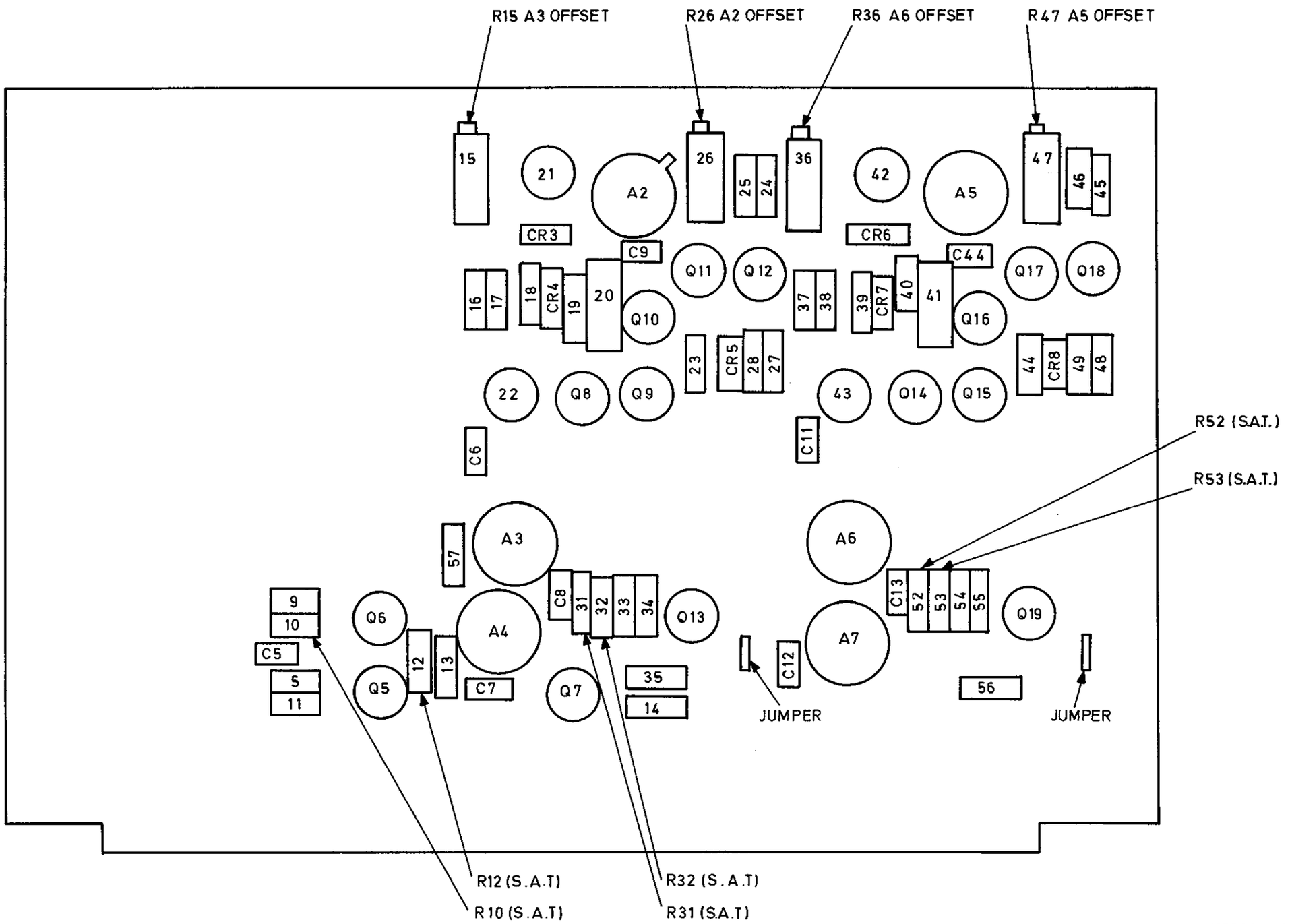

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Figure 1-19. Signal Conditioning Board, Component Location Diagram

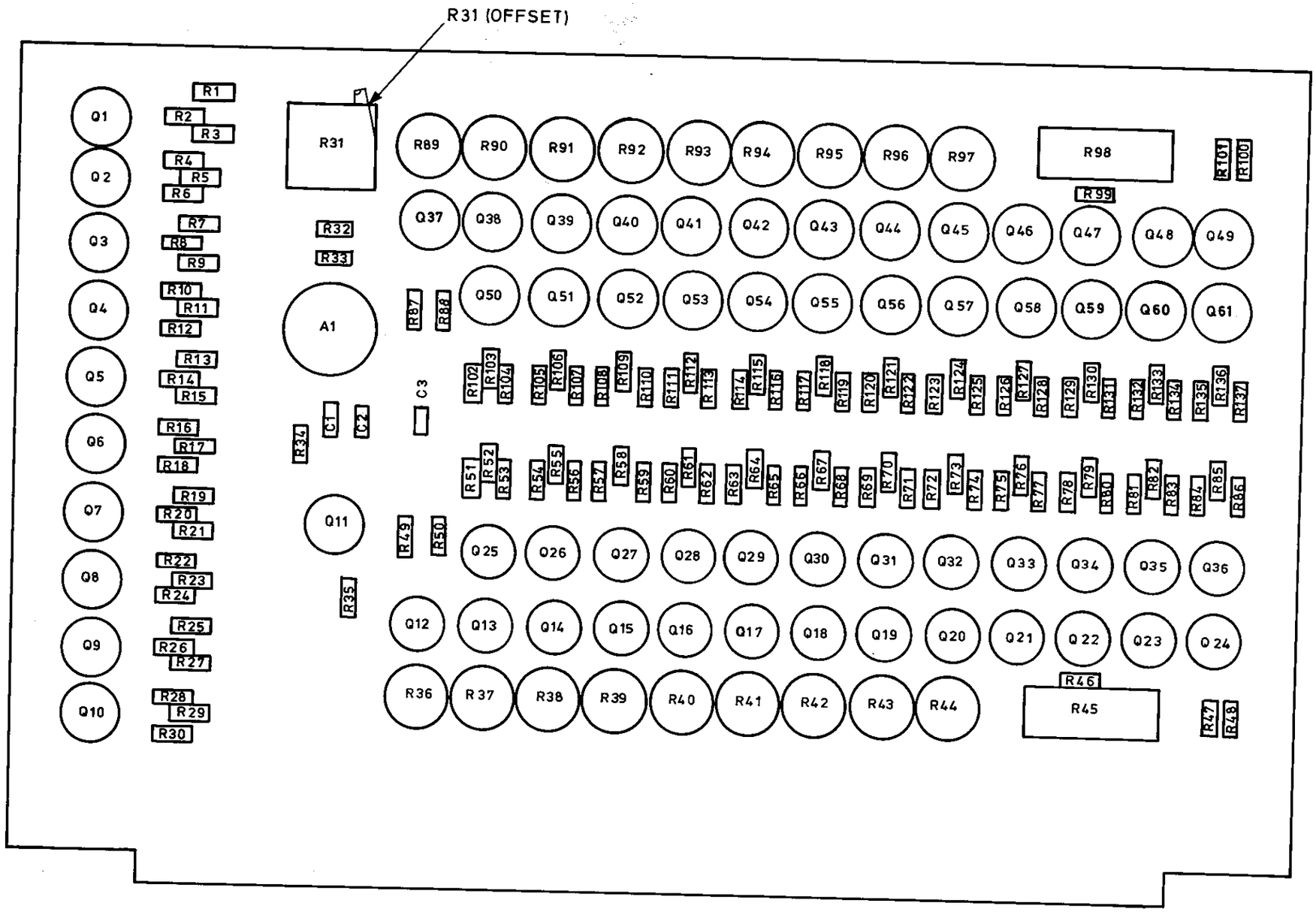

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Figure 1-20. Sin/Cos Network Board, Component Location Diagram

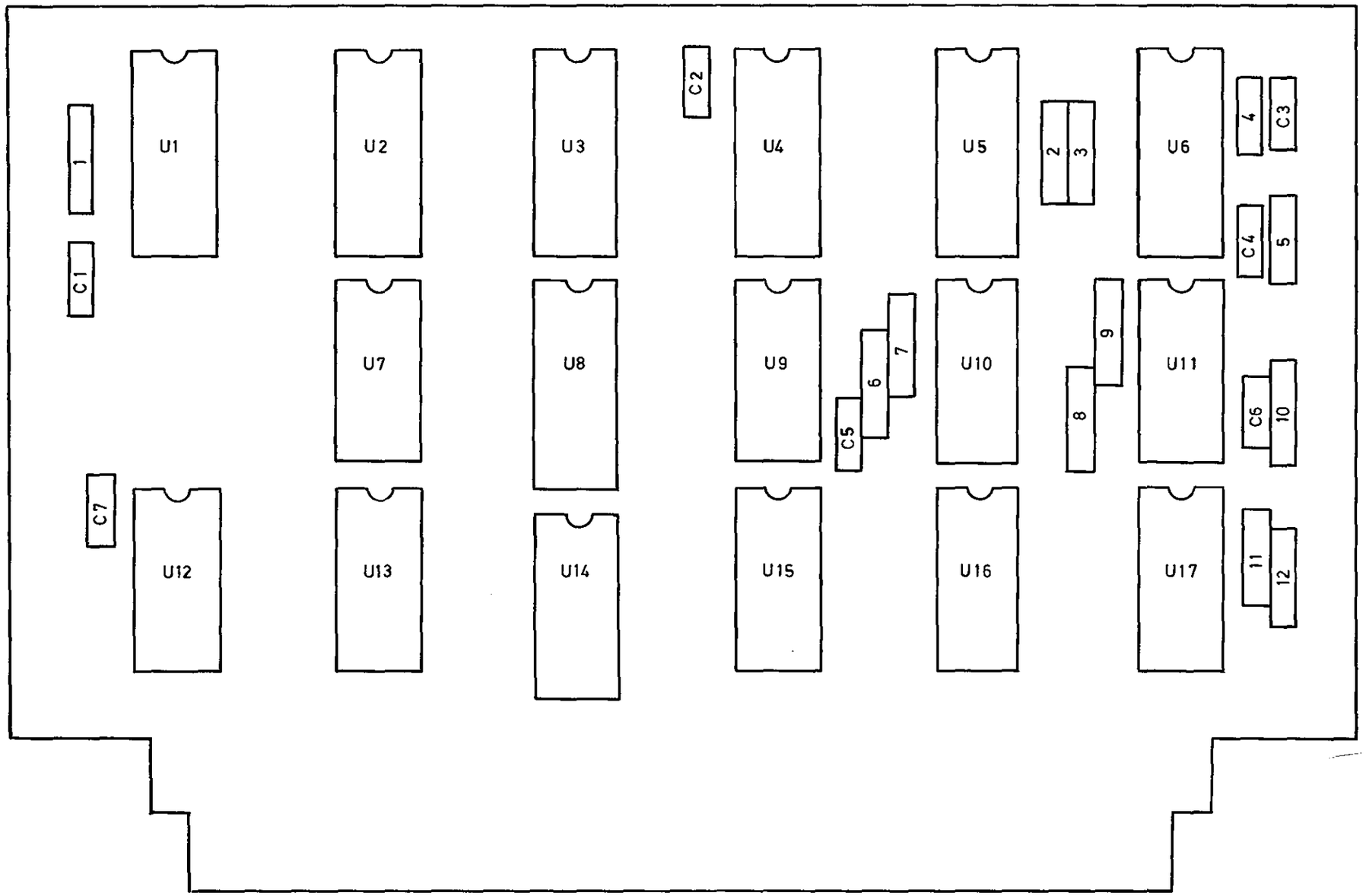

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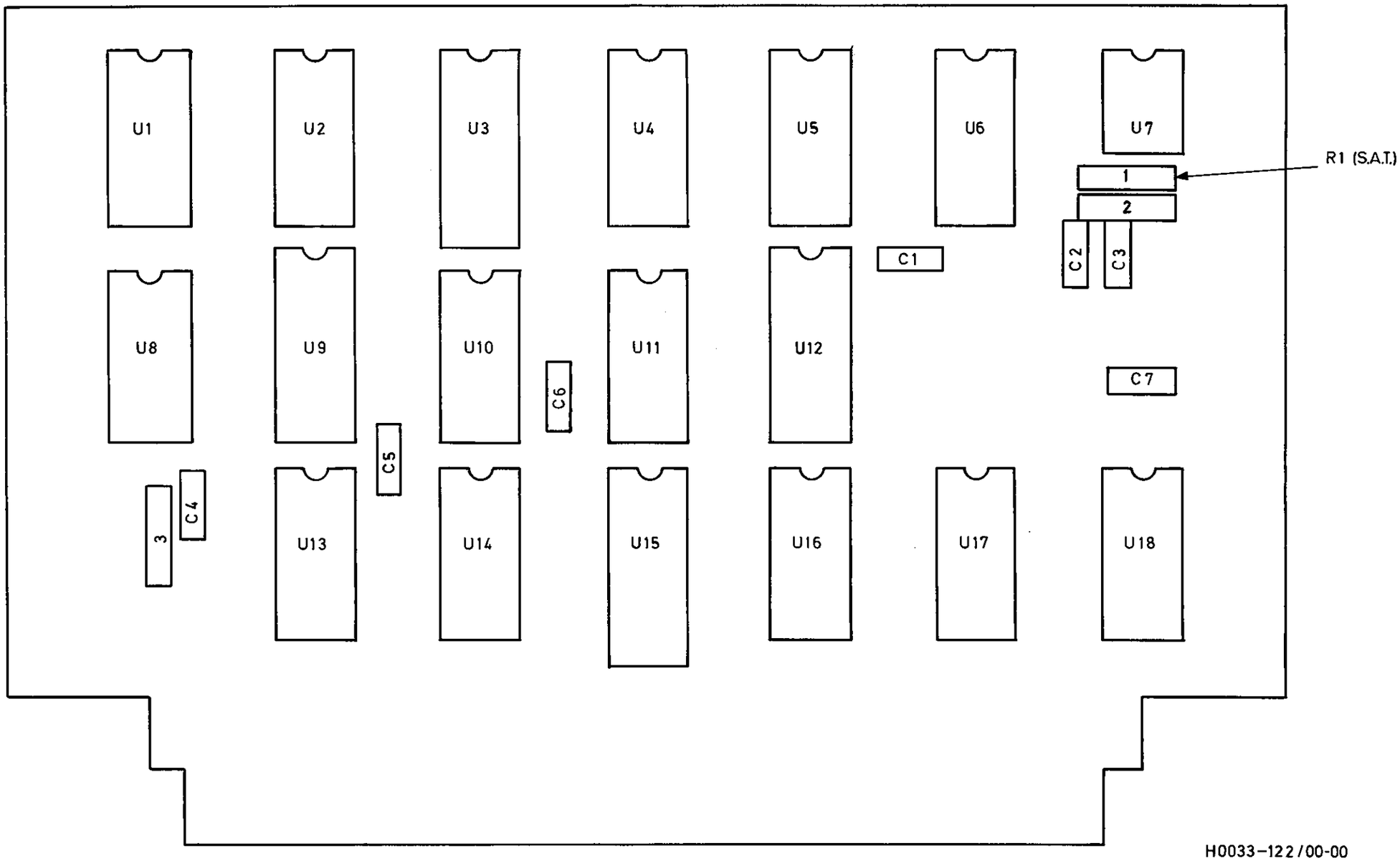
Figure 1-21. Successive Approximation Board, Component Location Diagram



H0033-122/00-00

Figure 1-22. Address/Combination Board, Component Location Diagram

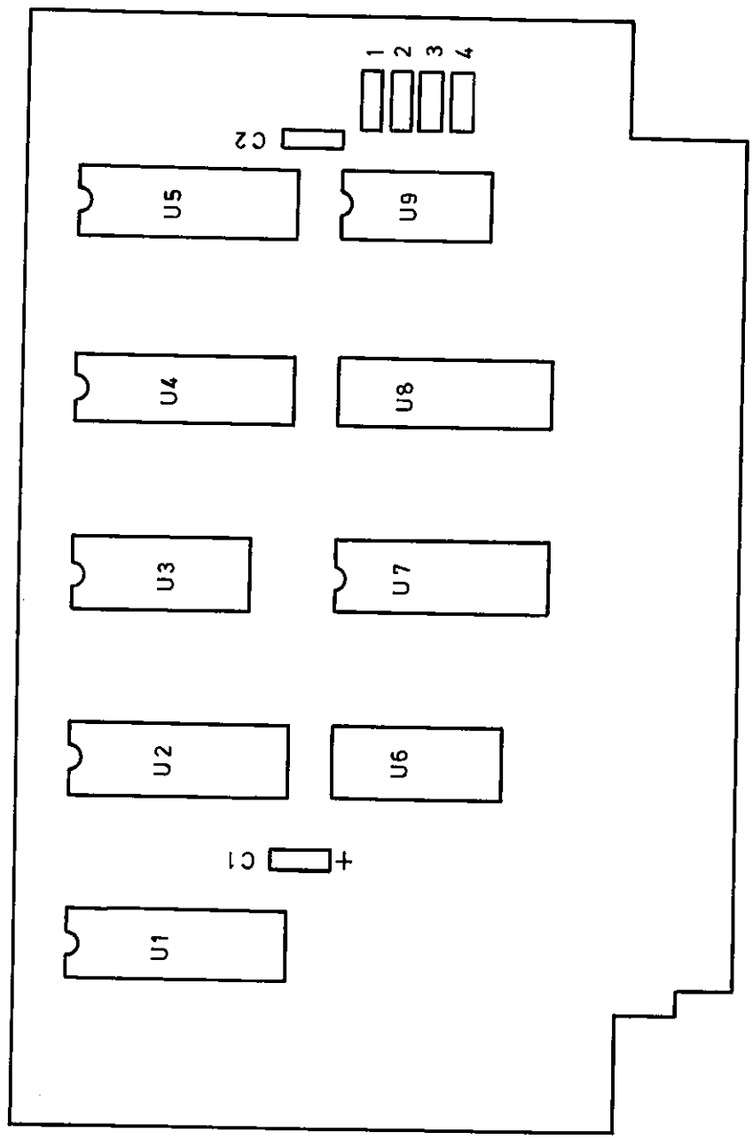


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Figure 1-23. Dual Output Registers Board, Component Location Diagram

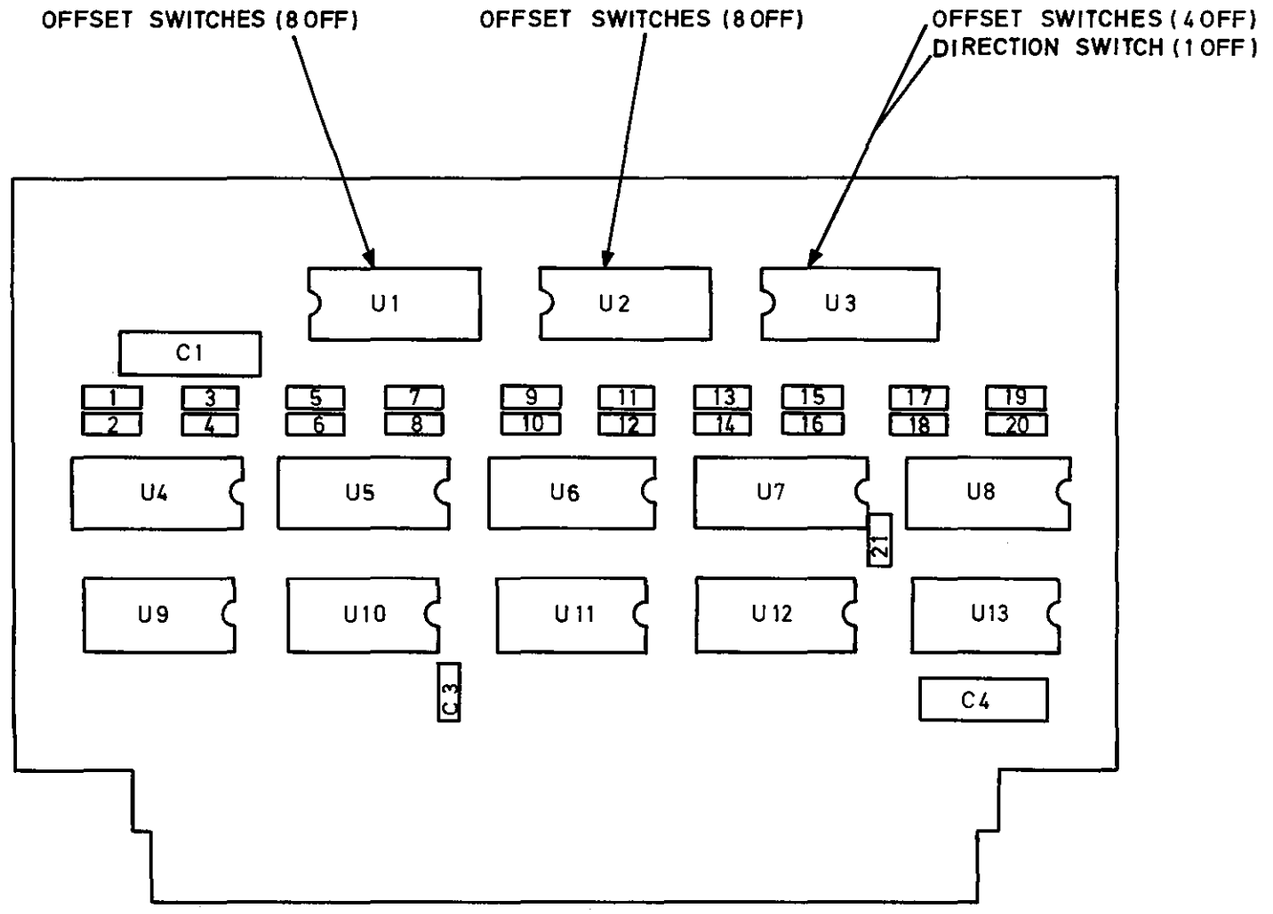

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Figure 1-24. Adder/Complementer Board, Component Location Diagram

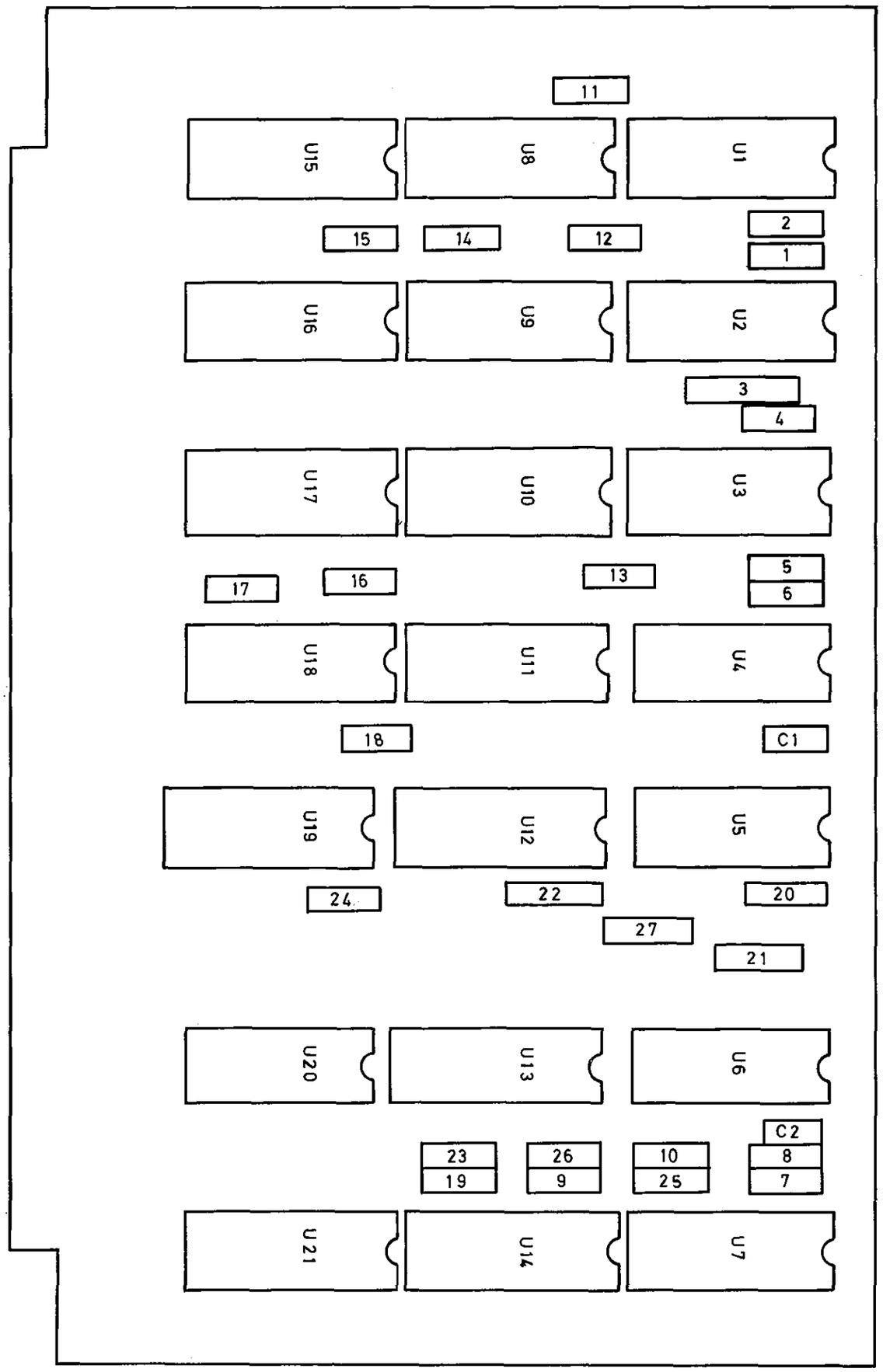

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Figure 1-25. Binary/BCD 10^2 to 10^{-2} Decades Board, Component Location Diagram

NATO UNCLASSIFIED

1-64 SGT3012-2

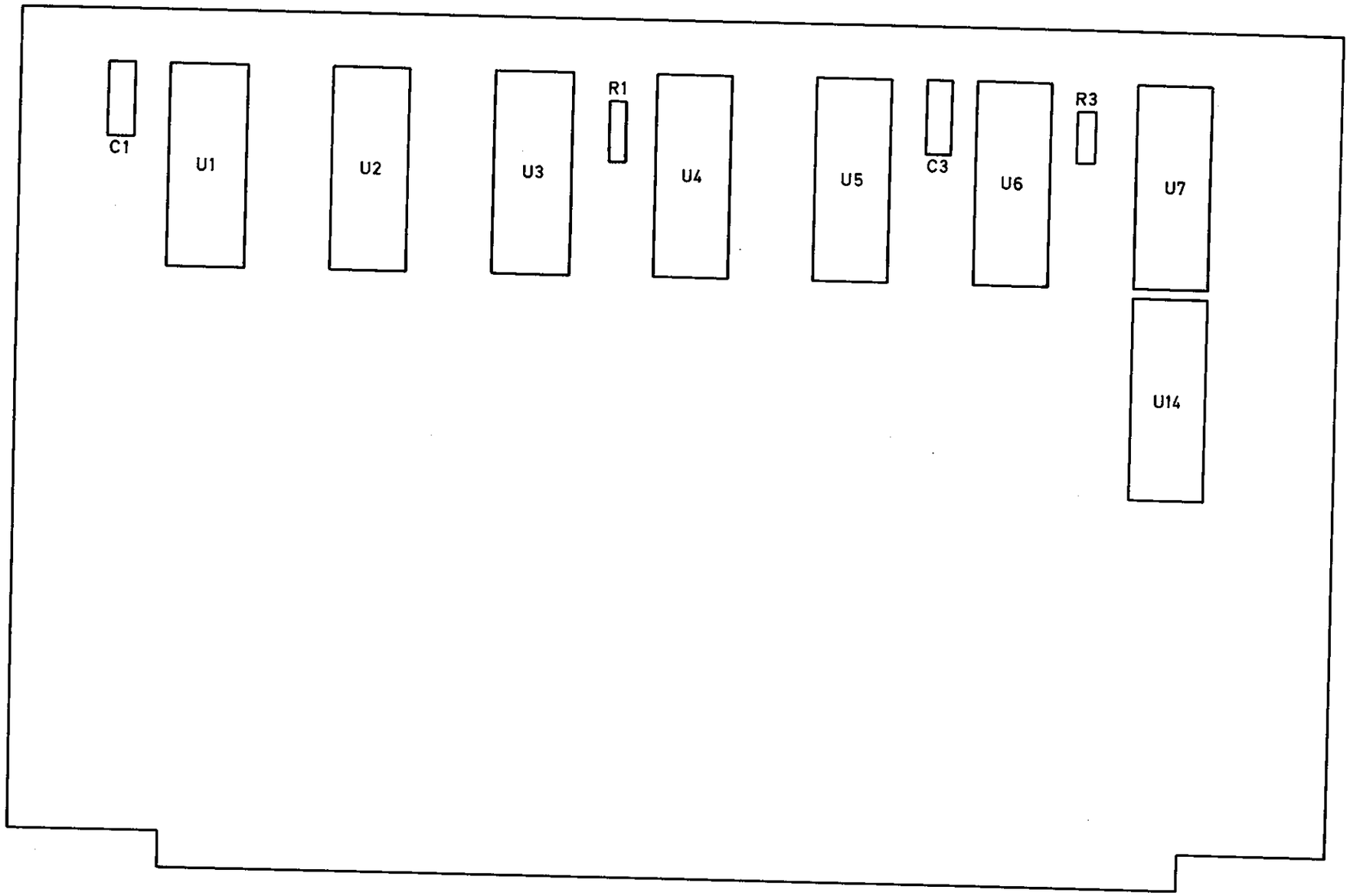

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Figure 1-26. Binary/BCD 10^{-3} Decade Board, Component Location Diagram

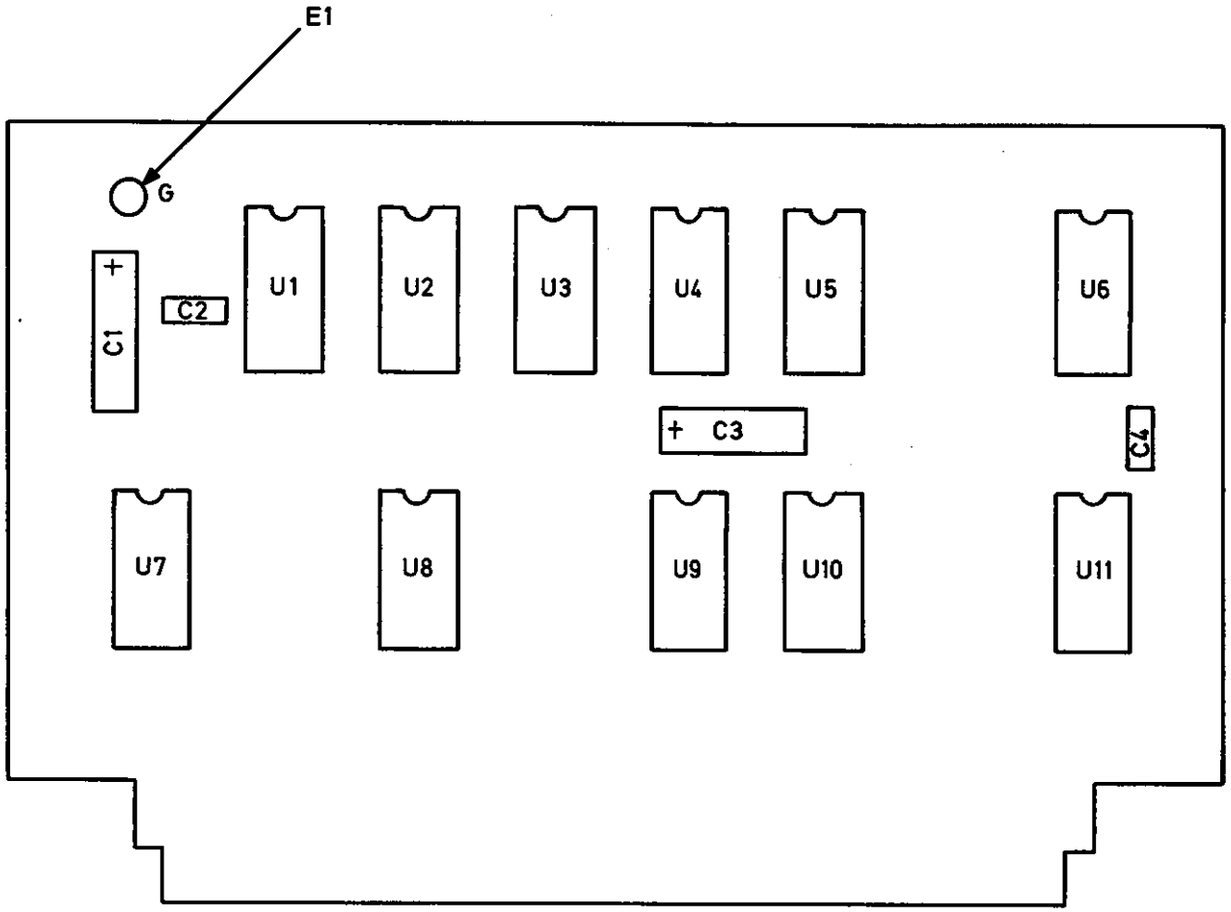

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Figure 1-27. Differential Line Driver Board, Component Location Diagram

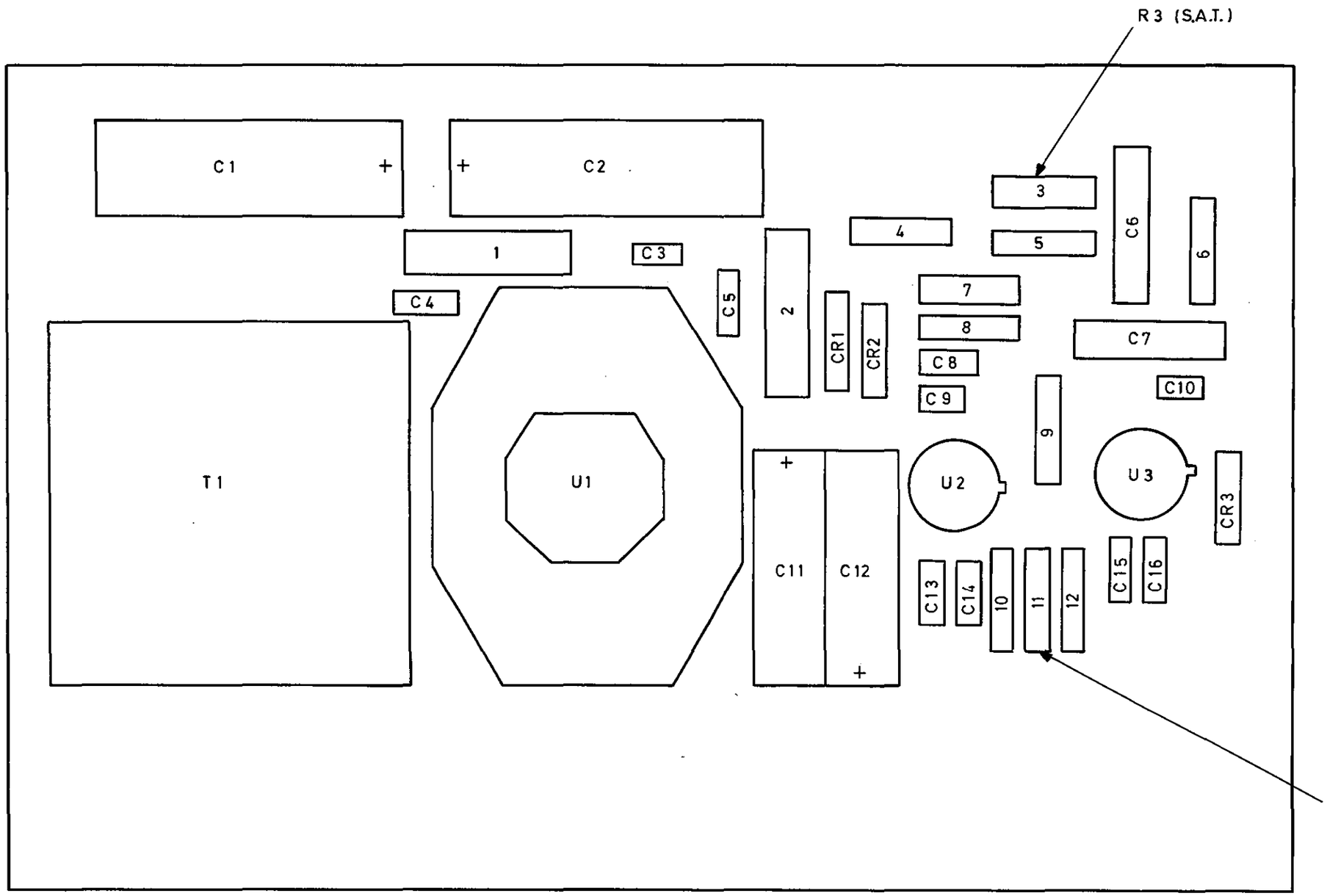
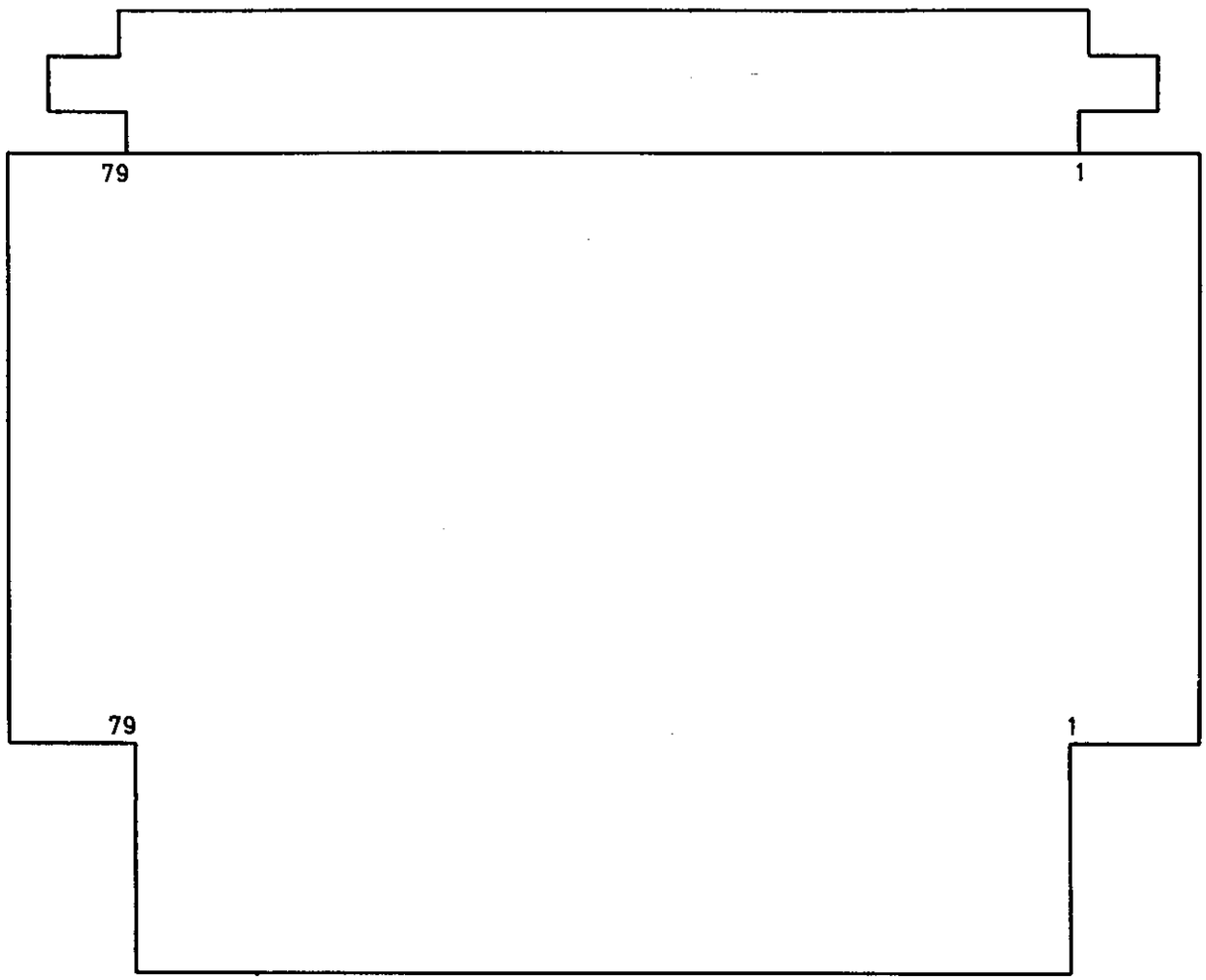


Figure 1-28. 1200 Hz Oscillator Board, Component Location Diagram



H0033-129/00-00

Figure 1-29. Extender Board (80-way), Component location Diagram

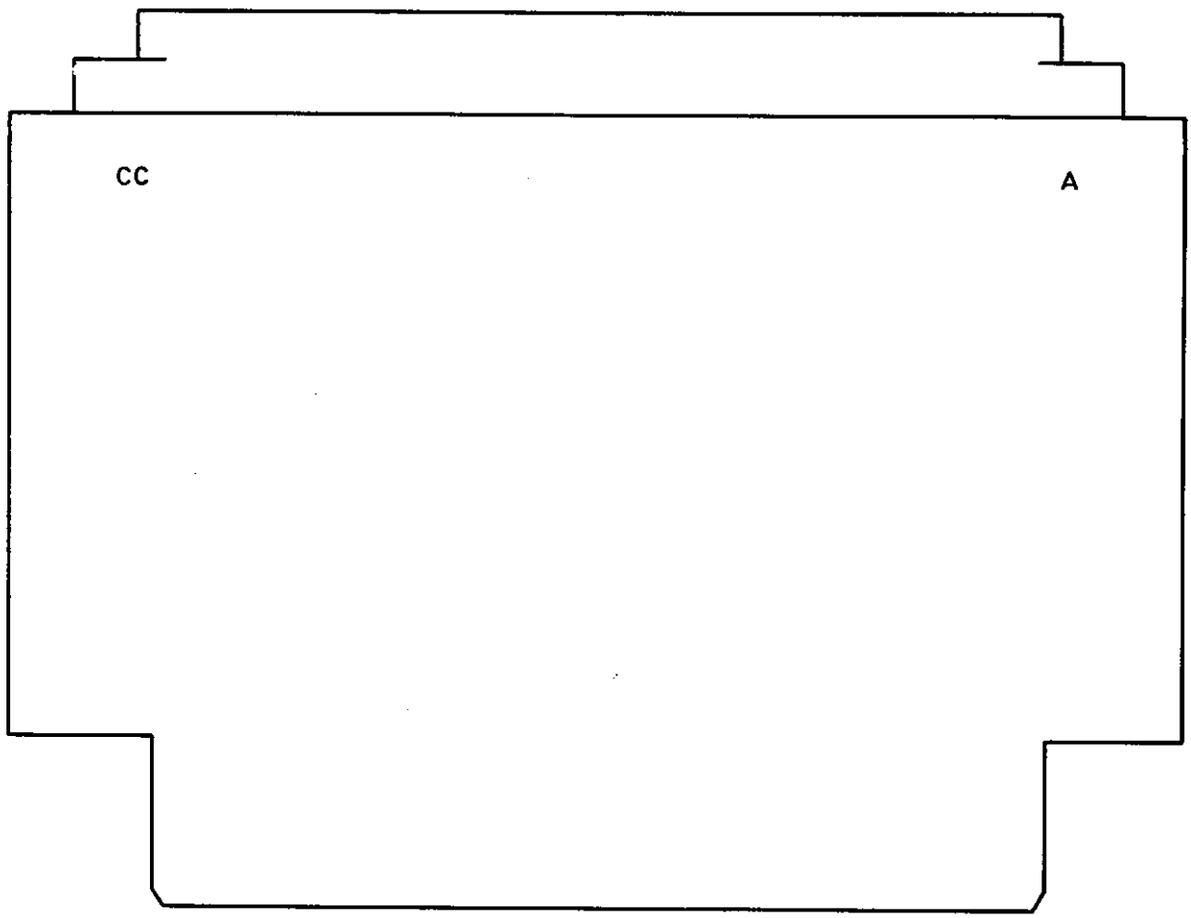


Figure 1-30. Extender Board (50-way), Component Location Diagram

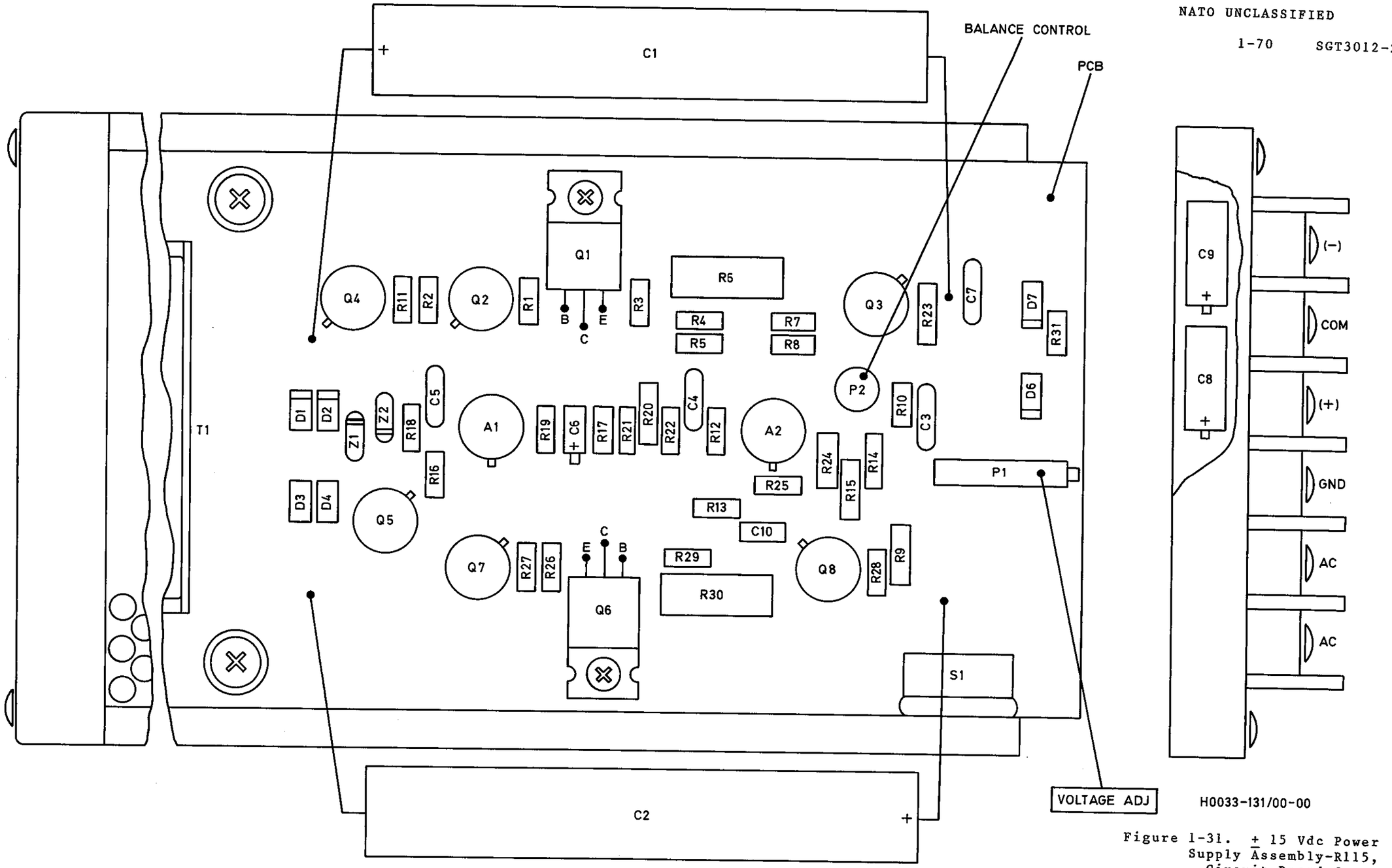
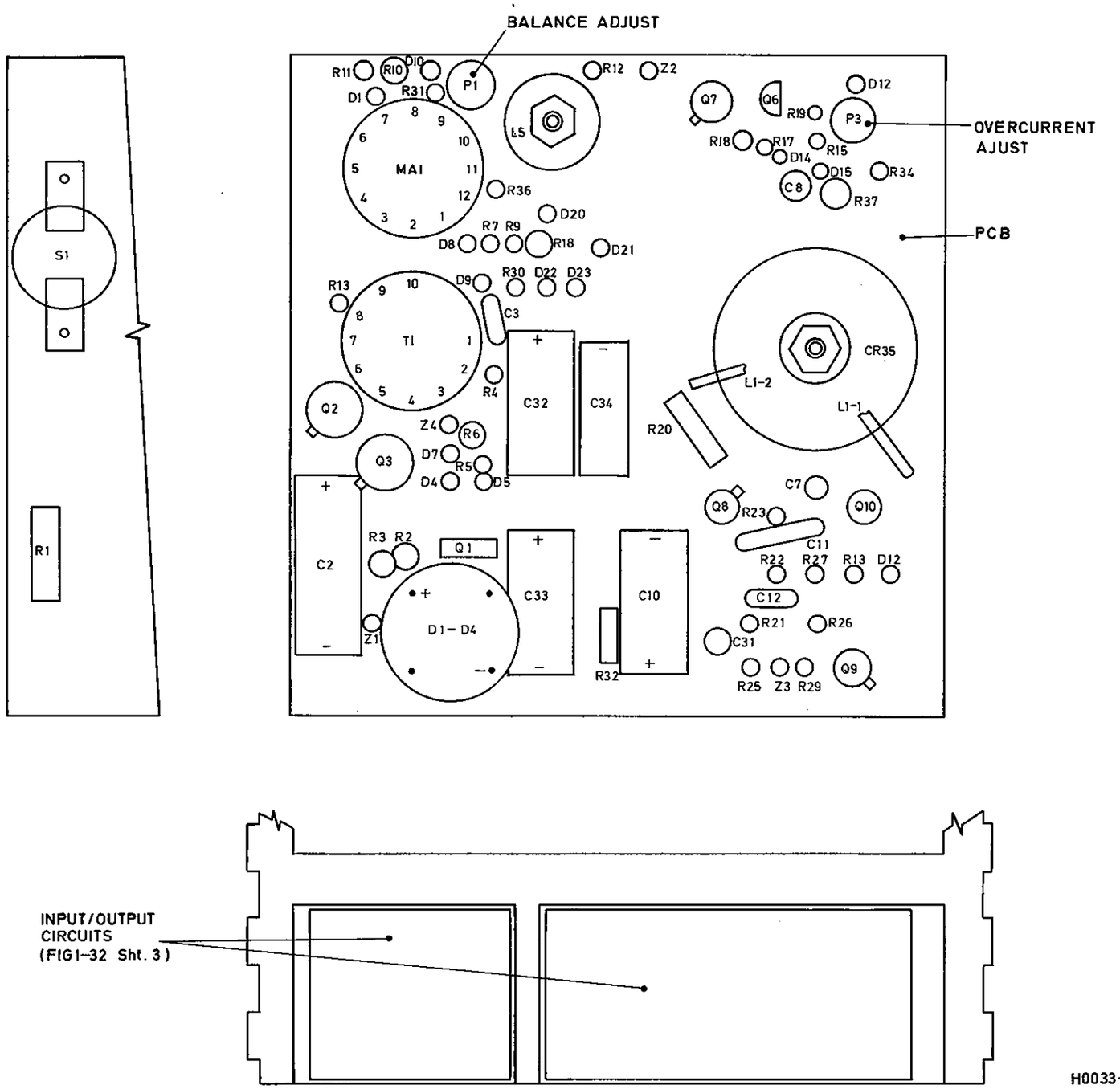
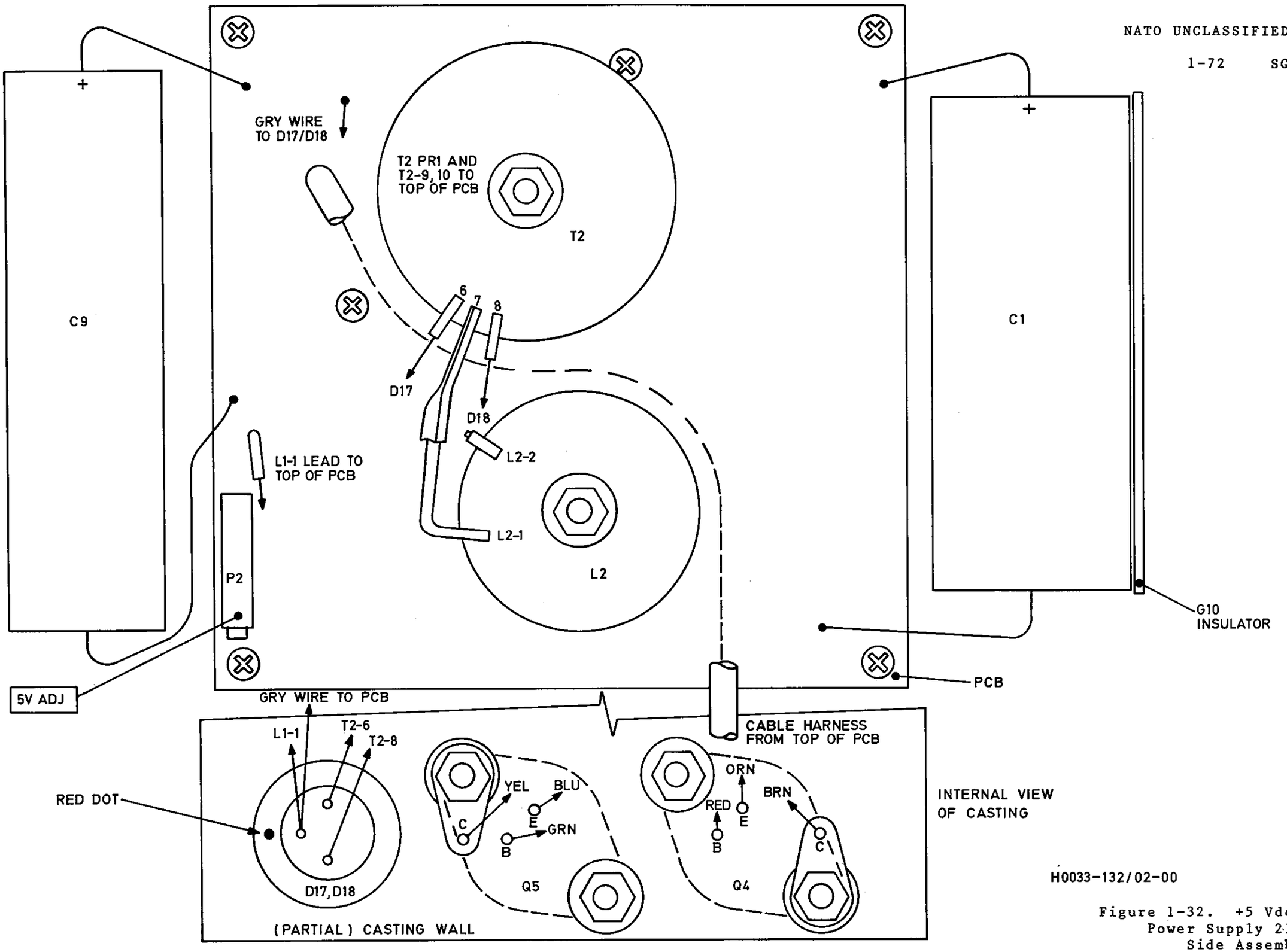


Figure 1-31. ± 15 Vdc Power Supply Assembly-R115, Circuit Board Component Location Diagram



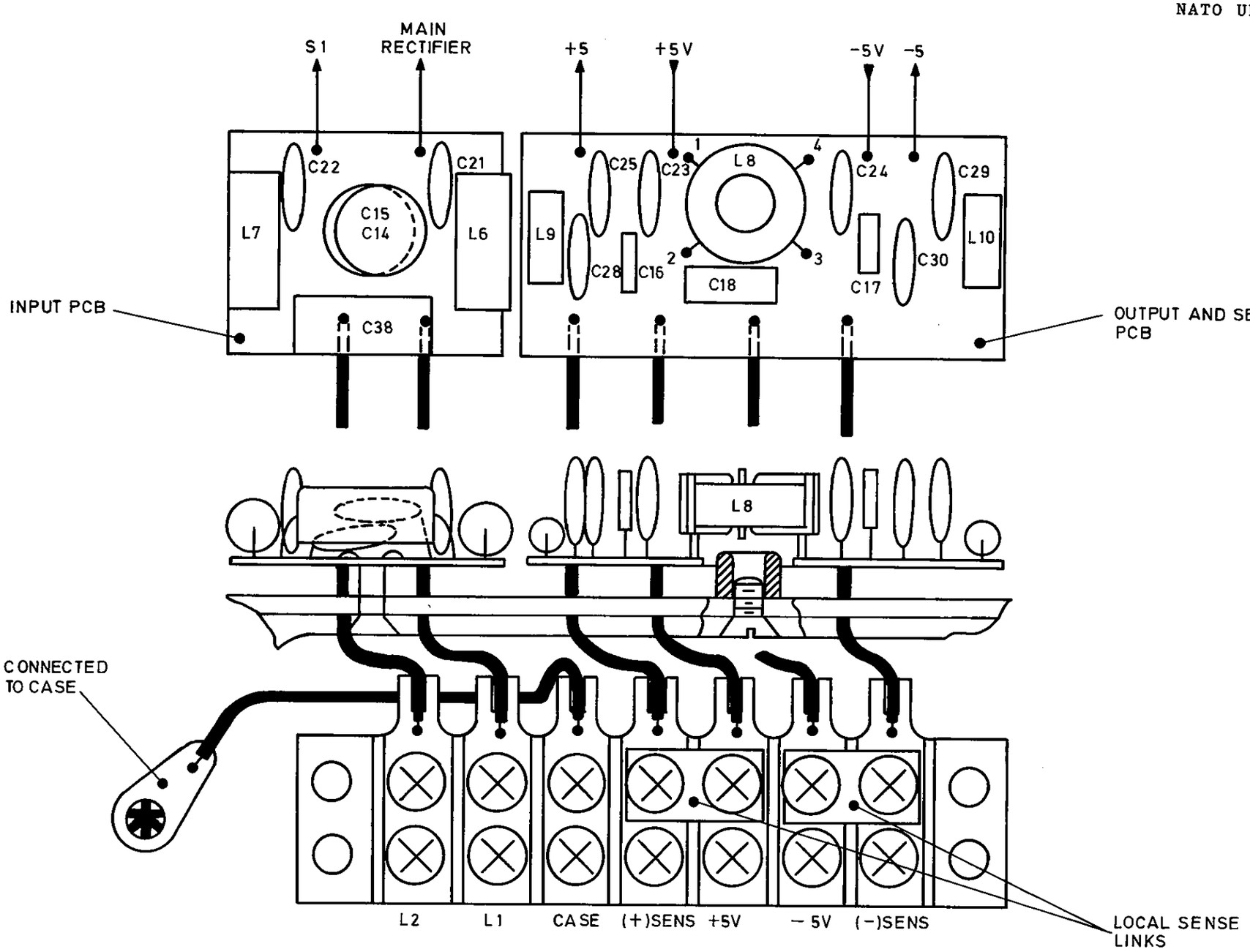
H0033-132/01-00

Figure 1-32. +5 Vdc Power Power Supply 210, Top Side Assembly and Component Location Diagram (Sheet 1)



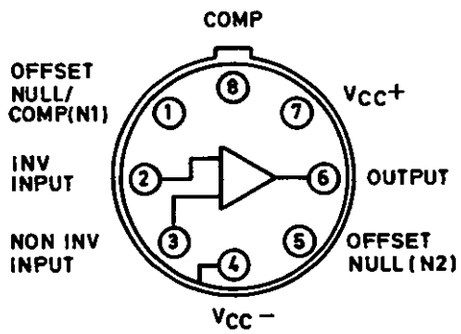
H0033-132/02-00

Figure 1-32. +5 Vdc Power Power Supply 210, Top Side Assembly and Component Location Diagram (Sheet 2)



H0033-132/03-00

Figure 1-32. +5 Vdc Power Power Supply 210, Top Side Assembly and Component Location Diagram (Sheet 3)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

PIN DESIGNATIONS

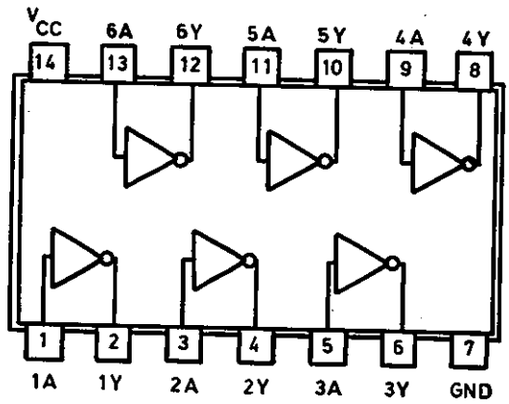
ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE $V_{CC}+$	+22V
SUPPLY VOLTAGE $V_{CC}-$	-22V
DIFFERENTIAL INPUT VOLTAGE (NON INVERTING INPUT WITH RESPECT TO INVERTING INPUT)	±30V
INPUT VOLTAGE	±15V

H0033-133/00-00

H0033-133/00-00

Figure 1-33. Operational Amplifier LM101A



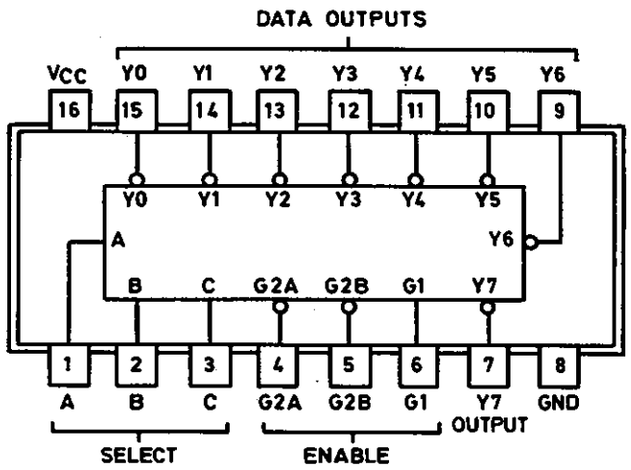
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	6·6 mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-134/00-00

Figure 1-34. Hex Inverters SN5404 and SN7404



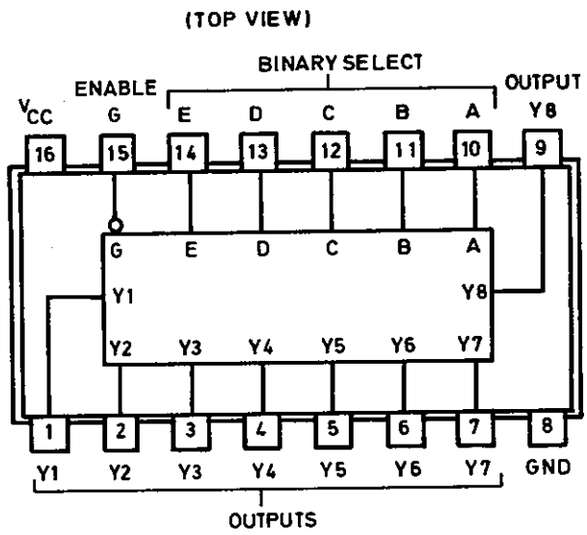
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	10 mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-135/00-00

Figure 1-35. Decoder/ Demultiplexer SN74LS138

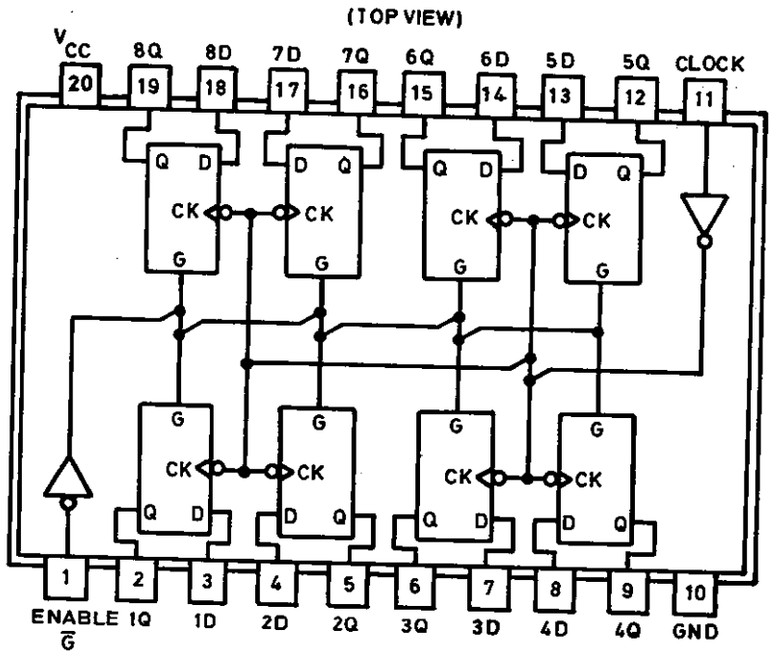


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	99mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·8V DC
OUTPUT VOLTAGE AT LOGIC1	5·0V DC
OUTPUT VOLTAGE AT LOGIC 0	0·4 V DC

H0033-136/00-00

Figure 1-36. Binary/BCD Converters SN54185 and SN74185

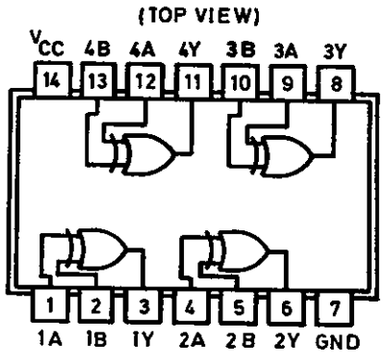


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	28mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·8V DC
OUTPUT VOLTAGE AT LOGIC 1	3·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·5V DC

H0033-137/00-00

Figure 1-37. Octal, Hex and Quad D-Type Flip-Flop SN54LS377

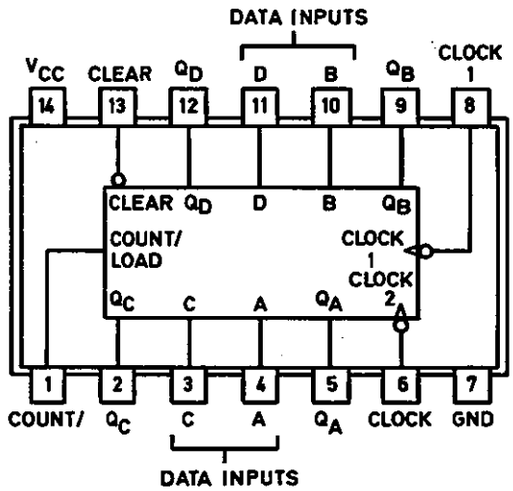


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5 V DC
SUPPLY CURRENT	10 mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·8 V DC
OUTPUT VOLTAGE AT LOGIC 1	5·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·5V DC

H0033-138/00-00

Figure 1-38. Quad 2-Input Exclusive OR-Gate SN54136

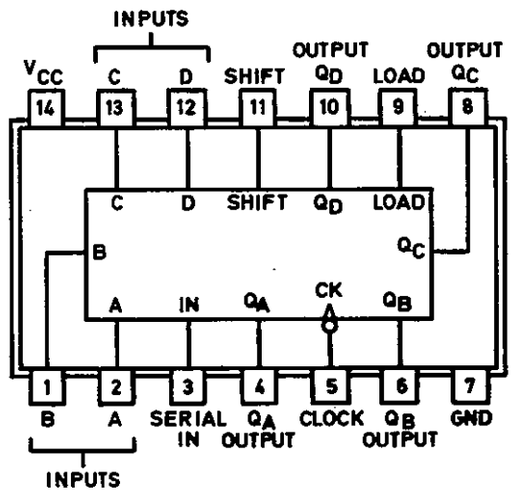


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5VDC
SUPPLY CURRENT	48mA
INPUT VOLTAGE AT LOGIC 1	2·0VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8VDC
OUTPUT VOLTAGE AT LOGIC 1	2·4VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4VDC

H0033-139/00-00

Figure 1-39. Presettable Binary Counter SN74177

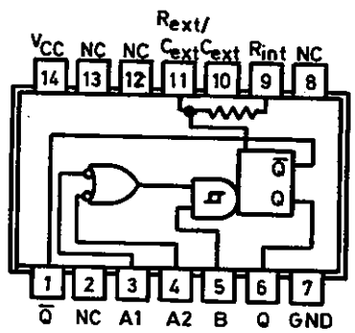


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5VDC
SUPPLY CURRENT	75mA
INPUT VOLTAGE AT LOGIC 1	2·0VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8VDC
OUTPUT VOLTAGE AT LOGIC 1	2·4VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4VDC

H0033-140/00-00

Figure 1-40. 4-Bit Parallel Access Shift Register SN74178

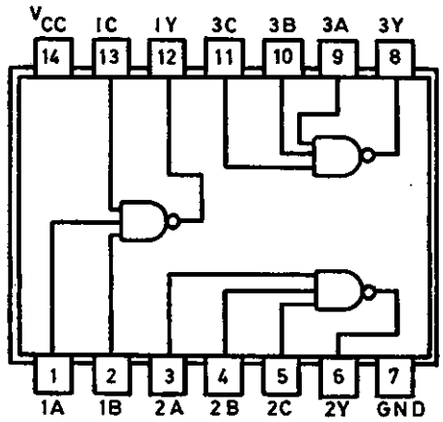


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	40 m A
INPUT VOLTAGE AT LOGIC 1	1·4 V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·8V DC
OUTPUT VOLTAGE AT LOGIC 1	2·4 V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4 V DC

H0033-141/00-00

Figure 1-41. Monostable Multivibrator SN74121



PIN DESIGNATIONS

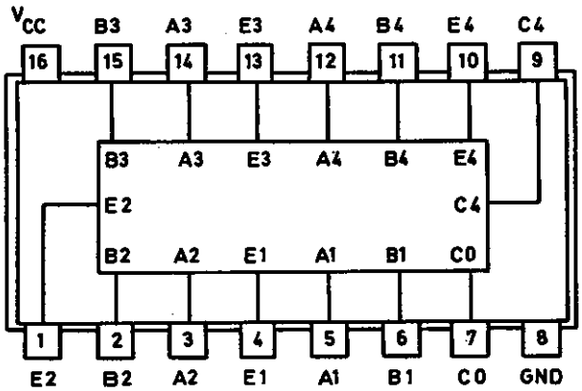
ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE V_{CC} +	5·5V DC
SUPPLY CURRENT	3·3mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-142/00-00

Figure 1-42. Triple 3-Input NAND-Gate SN74LS10

(TOP VIEW)

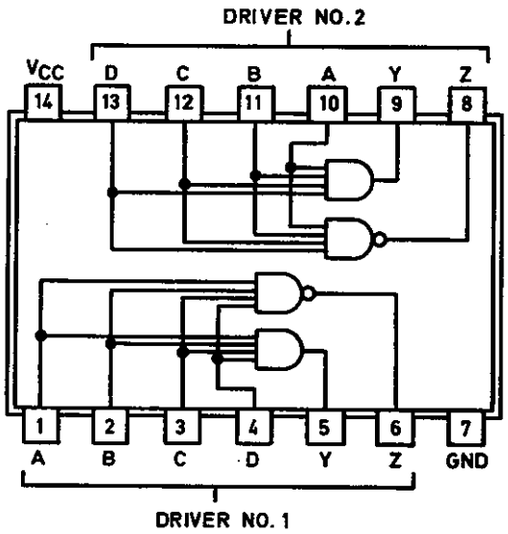


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	7·0 VDC
SUPPLY CURRENT	110 m A
INPUT VOLTAGE AT LOGIC 1	2·0 VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8 VDC
OUTPUT VOLTAGE AT LOGIC 1	2·4 VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4 VDC

H0033-143/00-00

Figure 1-43. 4-Bit Binary Full Adder SN54LS283

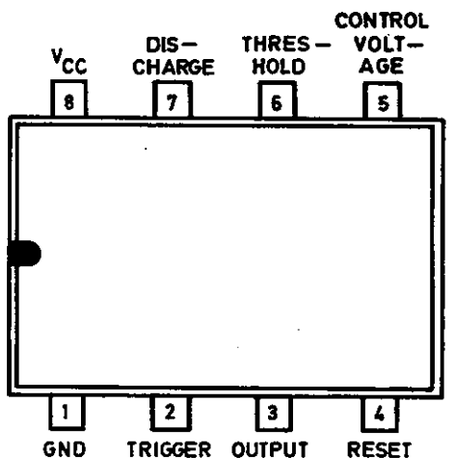


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5VDC
SUPPLY CURRENT	40mA
INPUT VOLTAGE AT LOGIC 1	2·0VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8VDC
OUTPUT VOLTAGE AT LOGIC 1	1·8VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4VDC

H0033-144/00-00

Figure 1-44. Dual Differential Line Driver SN75183

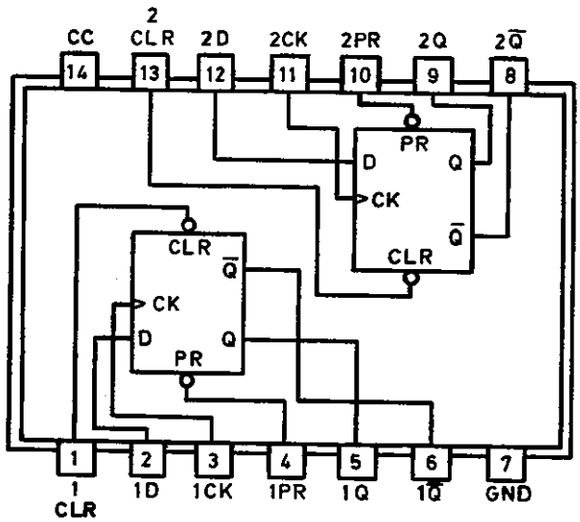


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	16 VDC
SUPPLY CURRENT	15 mA
TRIGGER VOLTAGE	5 VDC
CONTROL VOLTAGE	11 VDC
OUTPUT VOLTAGE AT LOGIC 1	13·3 VDC
OUTPUT VOLTAGE AT LOGIC 0	2·5 VDC

H0033-145/00-00

Figure 1-45. Precision Timer NE555



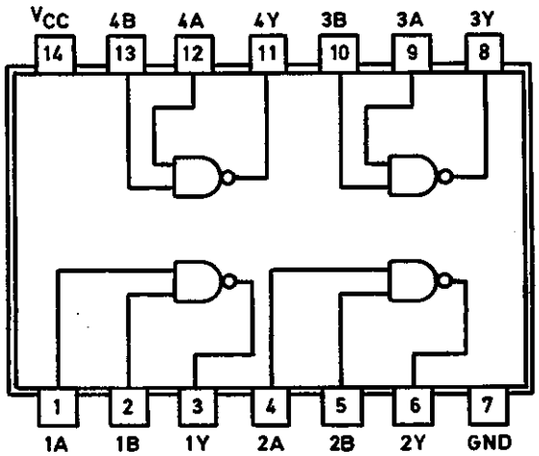
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5 V DC
SUPPLY CURRENT	8mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-146/00-00

Figure 1-46. Dual D-Type Flip-Flop SN5474



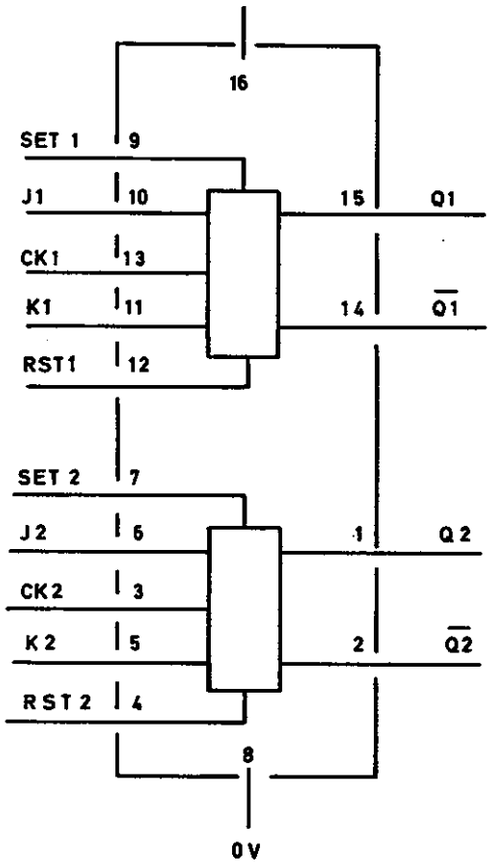
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE V_{CC+}	5·5V DC
SUPPLY CURRENT	4·4mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-147/00-00

Figure 1-47. Quad 2-Input Positive NAND-Gate SN7400

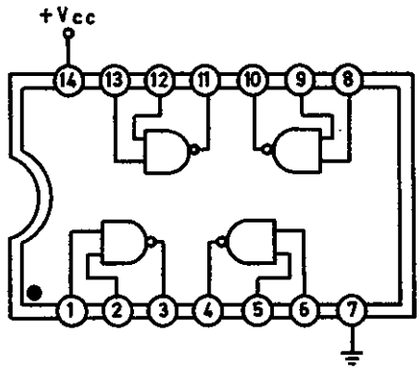


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	18 VDC
SUPPLY CURRENT	40 mA
INPUT VOLTAGE AT LOGIC 1	11 VDC
INPUT VOLTAGE AT LOGIC 0	4 VDC
OUTPUT VOLTAGE AT LOGIC 1	14·95 VDC
OUTPUT VOLTAGE AT LOGIC 0	0·5 VDC

H0033-148/00-00

Figure 1-48. Dual J-K Master-Slave Flip-Flop CD4027



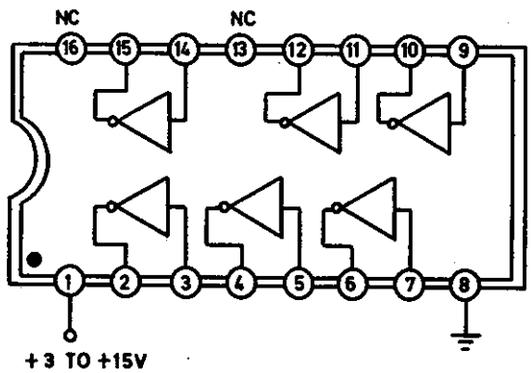
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	15V DC
SUPPLY CURRENT AT 5V 1MHz	0·4mA
INPUT VOLTAGE AT LOGIC 1	2.0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·8V DC
OUTPUT VOLTAGE AT LOGIC 1	2.4VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-149/00-00

Figure 1-49. Quad 2-Input NAND-Gate CD4011



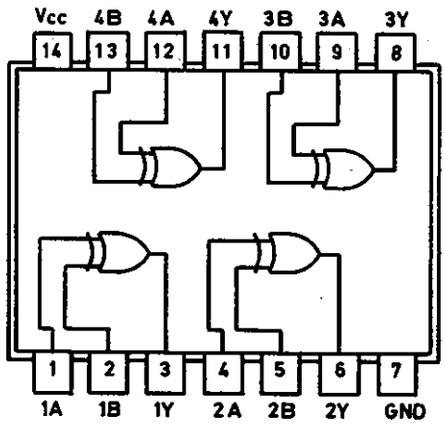
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	15VDC
SUPPLY CURRENT	2·5mA
INPUT VOLTAGE	10VDC
INPUT CURRENT	1·6mA
OUTPUT VOLTAGE	10VDC
OUTPUT CURRENT	1·6mA

H0033-150/00-00

Figure 1-50. Hex Buffer/ Converter CD4049



PIN DESIGNATIONS

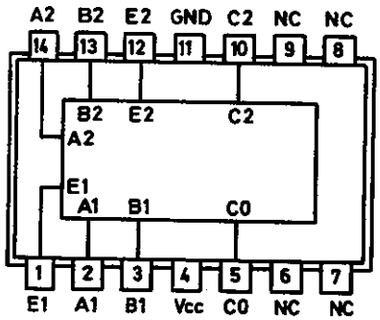
ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE Vcc+	5·5VDC
SUPPLY CURRENT	10mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5V DC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4V DC

H0033-151/00-00

Figure 1-51. Quad 2-Input Exclusive OR-Gate SN5486

(TOP VIEW)



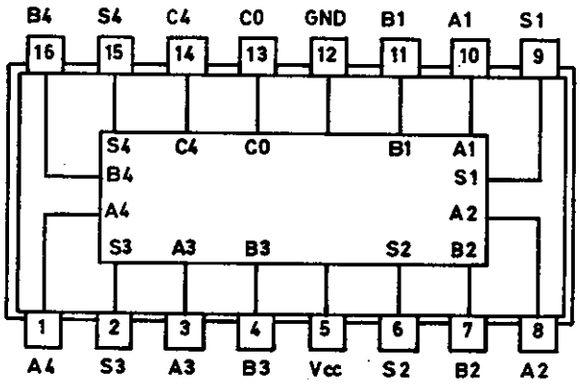
ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5 VDC
SUPPLY CURRENT	58mA
INPUT VOLTAGE AT LOGIC 1	2·0VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8VDC
OUTPUT VOLTAGE AT LOGIC 1	2·4 VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4VDC

H0033-152/00-00

Figure 1-52. 2-Bit Binary Full Adder SN7482

TOP VIEW

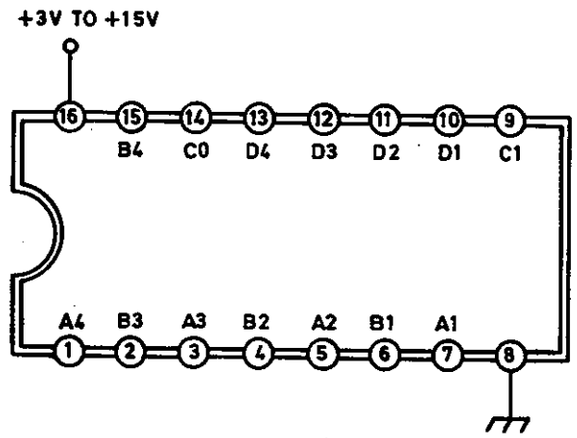


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5 VDC
SUPPLY CURRENT	110 mA
INPUT VOLTAGE AT LOGIC 1	2·0 VDC MIN
INPUT VOLTAGE AT LOGIC 0	0·8 VDC
OUTPUT VOLTAGE AT LOGIC 1	2·4 VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4 VDC

H0033-153/00-00

Figure 1-53. 4-Bit Binary Full Adder (Fast Carry) SN7483



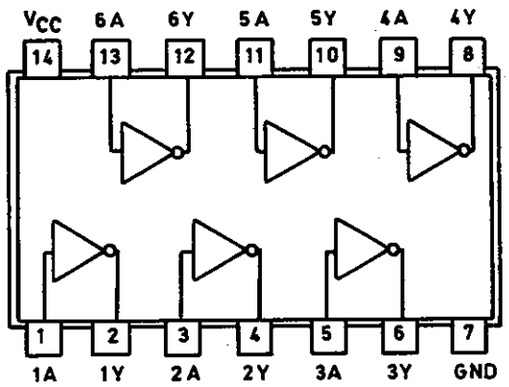
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	15V DC
SUPPLY CURRENT	4mA
INPUT VOLTAGE	10V
INPUT CURRENT	3·2mA
OUTPUT VOLTAGE	10V
OUTPUT CURRENT	3·2mA

H0033-154/00-00

Figure 1-54. 4-Bit Full Adder (Parallel Carryout) CD4008



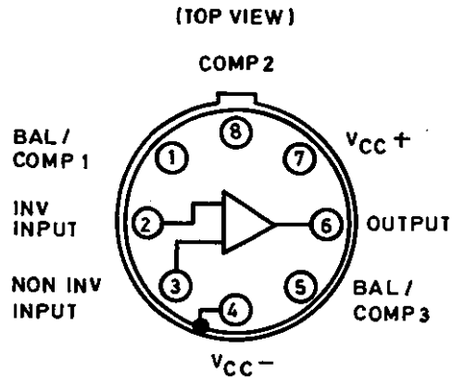
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	5·5V DC
SUPPLY CURRENT	6·6mA
INPUT VOLTAGE AT LOGIC 1	2·0V DC MIN
INPUT VOLTAGE AT LOGIC 0	0·7V DC
OUTPUT VOLTAGE AT LOGIC 1	2·5VDC MIN
OUTPUT VOLTAGE AT LOGIC 0	0·4VDC

H0033-155/00-00

Figure 1-55. Hex Inverter SN54LS04

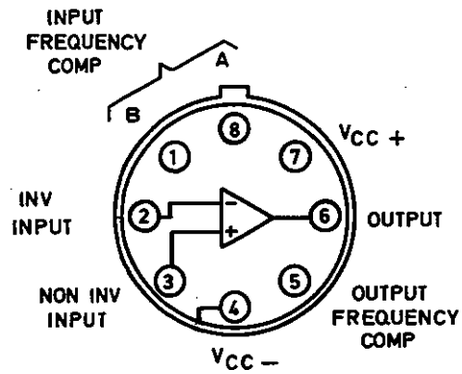


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	20 V DC
SUPPLY CURRENT	8m A
INPUT VOLTAGE	15 V DC
OUTPUT VOLTAGE SWING	26 V

H0033-156/00-00

Figure 1-56. GP Operational Amplifier LM118



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

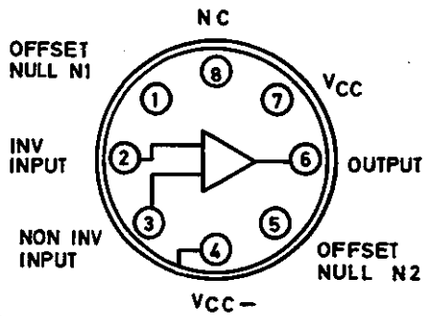
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE V_{CC}+	+18V DC
SUPPLY VOLTAGE V_{CC} -	−18V DC
DIFFERENTIAL INPUT VOLTAGE (NON INVERTING INPUT WITH RESPECT TO INVERTING INPUT)	±5V DC
INPUT VOLTAGE	±10V DC

H0033-157/00-00

Figure 1-57. Linear Operational Amplifier uA 709



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

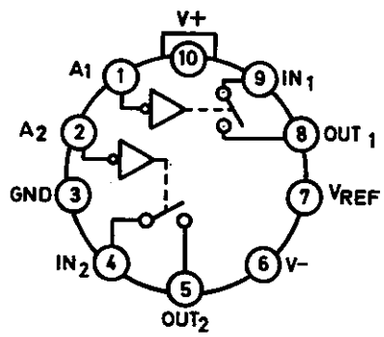
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE $V_{CC}+$	+22V DC
SUPPLY VOLTAGE $V_{CC}-$	−22V DC
DIFFERENTIAL INPUT VOLTAGE (NON INVERTING INPUT WITH RESPECT TO INVERTING INPUT)	±30V DC
INPUT VOLTAGE	±15V DC

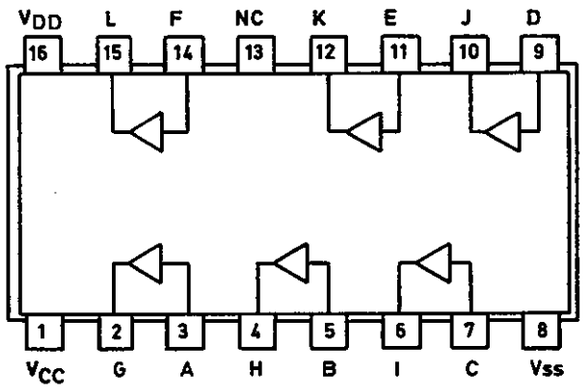
H0033-158/00-00

Figure 1-58. Linear Operational Amplifier uA 741



H0033-159/00-00

Figure 1-59. SPST Analogue Switch H12-200

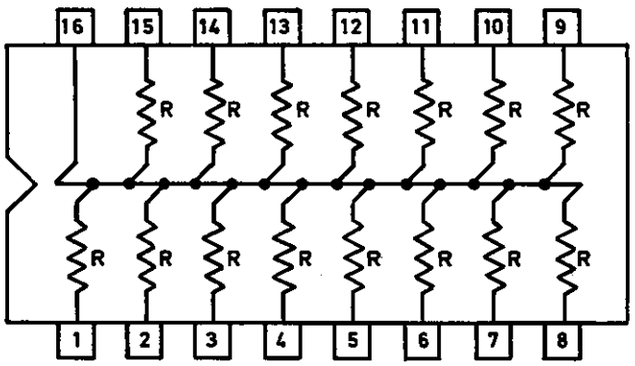


ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	18 VDC
SUPPLY CURRENT	45mA
INPUT VOLTAGE AT LOGIC 1	11 VDC
INPUT VOLTAGE AT LOGIC 0	4·0V DC
OUTPUT VOLTAGE AT LOGIC 1	15 VDC
OUTPUT VOLTAGE AT LOGIC 0	0·05V DC

H0033-160/00-00

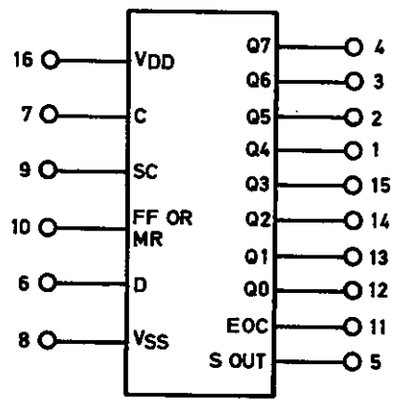
Figure 1-60. Hex Buffer/ Converter CD4010



PIN DESIGNATIONS

H0033-161/00-00

Figure 1-61. Resistive Network 898-1-R



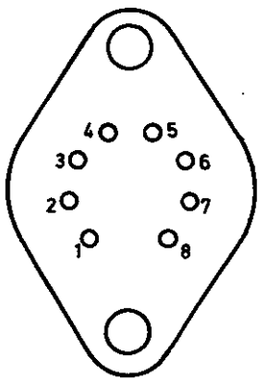
PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	18VDC
SUPPLY CURRENT	100mA
INPUT VOLTAGE AT LOGIC 1	11VDC
INPUT VOLTAGE AT LOGIC 0	4VDC
OUTPUT VOLTAGE AT LOGIC 1	14·95VDC
OUTPUT VOLTAGE AT LOGIC 0	0·05VDC

H0033-162/00-00

Figure 1-62. Successive Approximation Registers MC14549 and MC14559



PIN DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE	18 V DC
SUPPLY CURRENT	3·5mA
INPUT VOLTAGE	15 V DC
OUTPUT VOLTAGE SWING	24V
OUTPUT CURRENT	2 A

H0033-163/00-00

Figure 1-63. GP Operational Amplifier (High Current) LH0021C

PART 2

MAINTENANCE AND REPAIR

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PART 2

SECTION I

PERFORMANCE TEST/FAULT ISOLATION

2.1 GENERAL

This section contains detailed instructions for offsite performance testing and fault isolation of each LRU of the angle encoder unit.

2.2 FACILITIES AND SUPPORT EQUIPMENT REQUIRED

Table 2-1 provides a listing of all tools, test jigs, facilities, and test equipment required for offsite maintenance of each LRU.

Table 2-1 Facilities and Support Equipment

Nomenclature	Model/Part No. or Specification No.	Qty
Angle Encoder Test Fixture	801628-1	1
10:1 Transducer	801681-4	1
Dial Assembly, 5-inch.	800239-13	1
BCD Display	516371	1
Power Supply	6114A-001	1
Oscilloscope	TEKTRONIX 7633-05	1
Vertical Amplifier, Plug-in.	TEKTRONIX 7A13	1
Dual Trace, Plug-in.	TEKTRONIX 7A26	2
Time Base, Plug-in.	TEKTRONIX 7B53A	1
Probe	TEKTRONIX P6101	5
Mutimeter, Digital (DMM).	FLUKE 8860A	1
Multimeter	AVO Model 8	1
Decade, Resistor	1434G	1
Counter, Electronic.	5345A-011	1
Load, Electronic	AC-DC ELECTRONICS EL-750B	1
Transformer	SUPERIOR ELECT 216B	1
Test Lead	POMONA B-48-0	2
Test Lead	POMONA B-48-2	2
Test Lead	POMONA 1370-48-0	2
Test Lead	POMONA 1370-48-2	2

Table 2-1 Facilities and Support Equipment (Continued)

Nomenclature	Model/Part No. or Specification No.	Qty
Test Lead	POMONA 3787-C-36	1
Test Lead	POMONA 3782-36-0	3
Test Lead	POMONA 3782-36-2	3
Test Lead	POMONA 3782-0	3
Test Lead	POMONA 3782-2	3
Power Cord	PACIFIC ELECTRICORD C-2114-03M-GY	1
Adaptor	3561-0	1
Adaptor	3561-2	1
Adaptor	3744	6

2.3 PERFORMANCE TEST/FAULT ISOLATION

The following paragraphs contain performance test procedures and fault isolation for each LRU and repairable sub-assembly.

Performance testing consists of checking the LRU under test against known performance standards to ensure that it meets the acceptable minimum specification. Procedural steps must be carried out in the given sequence; switch settings and meter readings must be made carefully to ensure accurate test results. Probable faults are diagnosed from the performance test results and by referring to the relevant functional block diagrams and schematic diagrams in part 1.

When under test, each LRU is made accessible by the use of Extender Board 212189-1 (80-way) or Extender Board 211300-1 (50-way) which are stowed in the Angle Encoder Unit in positions A19 and A20 respectively.

For test purposes, a standard test setup is required as shown in figure 2-1. Details of the special-to-type cables are shown in figure 2-2.

NOTE

When making 'in-circuit' resistance measurements or determining the value of SAT (select-at-test) resistors with the digital multimeter (DMM), use the low terminal connection method.

2.3.1 SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6 PERFORMANCE TEST PROCEDURES

Performance testing of the synchronous demodulator/multiplexer board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required

and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.1.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1	
Extender board 211300-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in, TEKTRONIX 7B53A	1 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Decade, Resistor, 1434G	1 reqd
Probe, TEKTRONIX P6101	5 reqd
Test lead POMONA 3782-36-0	3 reqd
Test lead POMONA 3782-36-2	3 reqd

b. Connect test setup as shown in figure 2-3 and insert extender board into position A1 or A2 in the angle encoder (figure 2-1) as required. Should also be made to figures 1-2 and 1-18.

c. Additional instructions are given in the procedural steps.

2.3.1.2 Step-by-Step Procedure. Table 2-2 provides a step-by-step procedure for checking the performance of the synchronous demodulator/multiplexer board.

Table 2-2 Synchronous Demodulator/Multiplexer Board P/N 212195-6, Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment and observe both oscilloscope screens.	E1,E2 E3,E4	Waveforms as shown in figure 2-4.	No waveforms: a. Using the oscilloscope check for 1200 Hz ± 13 V square wave on test point E5. b. 1200 Hz not present - check for 1200 Hz ± 10.5 V p-p sine wave on pin F.

Table 2-2 Synchronous Demodulator/Multiplexer Board P/N 212195-6, Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
				c. 1200 Hz present on pin F - trouble-shoot U9 and associated circuit. Not all wave-forms: a. Troubleshoot relevant input circuit(s) U2, U4,U6,U8. b. Use DMM and decade resistor to select value of SAT resistors. NOTE 1. U2,U4 have gain of 2 with 0-6.35 V p-p maximum input. 2. U6,U8 have gain of 1.3 with 0-10.89 V p-p maximum input.
2.	Using the oscilloscope, check outputs of U1,U3,U5,U7.	Pin 6 on each IC.	Unity gain.	No output - defective IC. Remove and replace as necessary. Incorrect level - check relevant resistor values using DMM. Remove and replace resistors as necessary. NOTE SAT resistors on pins 1 and 5 should be approx equal in value.

Table 2-2 Synchronous Demodulator/Multiplexer Board P/N 212195-6, Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
3.	Using the oscilloscope, check rectified output from each channel.	Q1,Q2 emitters. Q3,Q4 emitters. Q5,Q6 emitters. Q7,Q8 emitters.	Waveform as shown in figure 2-5a. (amplitude depends upon input levels and stage gains).	No output - both transistors in a pair are open-circuit. Remove and replace as necessary. Half-wave rectification observed - one transistor in a pair open-circuit. Remove and replace as necessary. Distortion observed - one or both transistors in a pair short-circuit. Remove and replace as necessary. NOTE Use DMM to check transistors for open and short-circuits.
4.	Using the oscilloscope and DMM, check the outputs of U10,U12,U13,U15.	E7,E8, E9,E6.	0 to $\pm$ 3 V (max). Ripple equal to or less than 5 milli-volts.	Troubleshoot defective circuit. NOTE: 1. COARSE maximum is just under 3 V. 2. FINE maximum is just over 3 V.
5.	Using the oscilloscope check MPLX SIN	Edge-pins 8 and J.	Waveform similar to that shown	Troubleshoot U11,U14 and associated circuits.

Table 2-2 Synchronous Demodulator/Multiplexer Board P/N 212195-6, Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
	and MPLX COS outputs.		in figure 2-5b. (Actual waveform depends upon input Maximum number of steps is 4 and the 'floor' ripple on each step should be equal to or less than 5 mV.	
6.	Using the DMM, check ELEV COS DC OUT output.	Edge-pin 16.	Same as voltage present on test point E6.	Check tracking on board. Repair as necessary.
7.	Using the oscilloscope, check SELECT COARSE and SELECT FINE inputs.	Edge-pins Y and 6.	TTL logic levels: 1=+2.4 to 5 Vdc. 0=0 to +0.5 Vdc.	
8.	Switch off test equipment and disconnect test setup.			

2.3.2 SIGNAL CONDITIONING BOARD P/N 206497-13 PERFORMANCE TEST PROCEDURES

Performance testing of the signal conditioning board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.2.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1	
Extender board 211300-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	4 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Decade, Resistor, 1434G	1 reqd
Test Lead POMONA 3782-0	3 reqd
Test Lead POMONA 3782-2	3 reqd

b. Connect test setup as shown in figure 2-6 and insert extender board into position A3 in the angle encoder (figure 2-1). Reference should also be made to figures 1-3, 1-4 and 1-19.

c. Additional instructions are given in the procedural steps.

2.3.2.2 Step-by-Step Procedure. Table 2-3 provides a step-by-step procedure for checking the performance of the conditioning board.

Table 2-3. Signal Conditioning Board P/N 206497-13 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment and monitor CLOCK waveform on the oscilloscope.	Edge-pins 10.	CLOCK waveform as shown in fig 1-3	Waveform not present: a. Using the oscilloscope check state of EC waveform. (pin 21). b. If EC is correct, troubleshoot Q5-Q7 and associated circuit. Use DMM and decade resistor to select SAT resistors R10, R12 if necessary.
2.	Using the oscilloscope, check SIN input.	Edge-pin X.	0 ± 4 V.	

Table 2-3. Signal Conditioning Board P/N 206497-13
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
3.	Using the oscilloscope, check SIN output.	Edge-pins 14 and R.	0 to -4 V.	No output: a. Using the oscilloscope, check for 0V ± 4 V on test point J. b. If correct - troubleshoot A2,Q10 and associated circuit. Polarity incorrect: a. Troubleshoot Q12, Q11, Q9, Q8 and associated circuits. b. Troubleshoot A4,Q13 and associated circuit. If necessary carry out calibration procedure described in Section V, Paragraph 2.16.1. c. If not correct troubleshoot A3 and associated circuit.
4.	Using the oscilloscope, check COS input.	Edge-pin Y.	0 ± 4 V.	
5.	Using the oscilloscope, check COS output.	Edge-pins 11 and M.	0 to +4 V.	No output: a. Using the oscilloscope, check for 0V ± 4 V on test point K.

Table 2-3. Signal Conditioning Board P/N 206497-13
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
				b. If correct - troubleshoot A5, Q16 and associated circuit. c. If not correct - troubleshoot A6 and associated circuit. Polarity incorrect: a. Troubleshoot Q18,Q17,Q15,Q14 and associated circuits. b. Troubleshoot A7,Q19 and associated circuit. If necessary carry out calibration procedure described in Section V, paragraph 2.16.1.
6.	Using the DMM measure the amplitude difference between the SIN input and SIN output.	Edge-pin X. Edge-pins 14 and R.	Equal to or less than 1 mV.	
7.	Using the DMM, measure the amplitude difference between the COS input and COS output.	Edge-pin Y. Edge-pins 11 and M.	Equal to or less than 1 mV.	
8.	Using the DMM measure the amplitude difference between the	Edge-pins 14 and R.	Equal to or less than 1 mV.	

Table 2-3. Signal Conditioning Board P/N 206497-13
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
	SIN output and COS output.	Edge-pins 11 and M.		
9.	Switch off test equipment and disconnect test setup.			

2.3.3 SIN/COS NETWORK BOARD P/N 206499-1 PERFORMANCE TEST PROCEDURES

Performance testing of the SIN/COS network board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.3.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.	
Extender board 211300-1.	1 reqd
Oscilloscope TEKTRONIX 7633-05.	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A.	1 reqd
Probe, TEKTRONIX P6101	5 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	2 reqd
Test Lead, POMONA 3782-2	2 reqd

b. Connect test setup as shown in figure 2-7 and insert extender board into position A4 in the angle encoder (figure 2-1). Reference should also be made figures 1-6 and 1-20.

c. Additional instructions are given in the procedural steps.

2.3.3.2 Step-by-Step Procedure. Table 2-4 provides a step-by-step procedure for checking the performance of the SIN/COS network board.

Table 2-4 SIN/COS Network Board, P/N 206499-1
Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	With power off, use DMM to check values of resistors in suspect SIN or COS ladder.			Remove and replace defective resistors as necessary.
2.	With power off, use DMM to check 'back-to-front' ratio of transistors in suspect SIN or COS ladder.			Remove and replace defective transistors as necessary.
3.	Switch on test equipment.			
4.	Using the oscilloscope, check logic level of inputs $2^{1}X$ to $2^{11}X$ and $\overline{2^{11}}$.			
5.	Using the oscilloscope, confirm that logic 1 levels have gated transistors 'on' and logic 0 levels have gated transistors 'off).	Transistor collectors	OFF=0 to +0.5 V. ON=+2.4 to +5 V.	Remove and replace defective transistors as necessary.
6.	Rotate 5-inch DIAL ASSEMBLY so that logic 0 is applied to transistors that had logic 1 inputs in step 5 and vice versa.			

Table 2-4 SIN/COS Network Board, P/N 206499-1
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
7.	Repeat step 5.		As step 5.	As step 5.
8.	Using the oscilloscope, monitor the output of the SIN/COS ladder network.	Edge-pin 18.	Waveforms similar to that shown in figure 2-8 with only those points active which correspond to $2^{1}X$ to $2^{11}X$ and 2^{12}.	
9.	Leave oscilloscope connected as in step 8 and, using another probe, monitor the output of A1.	A1-6.	Observe output of +14 V (max) for each input of step 8.	Troubleshoot A1 and associated circuit. NOTE R31 should be calibrated if A1 is replaced. (Refer to section V, paragraph 2.16.2).
10.	Leave oscilloscope connected as in steps 8 and 9, and using another probe, monitor the COMP OUT signal.	Edge-pin 20.	Observe levels of +5 V when Q11 is 'off' and 0V to to +0.7 V when Q11 is 'on'.	Troubleshoot Q11 and associated circuit.
11.	Switch off test equipment and disconnect test setup.			

2.3.4 SUCCESSIVE APPROXIMATION BOARD P/N 206498-1 PERFORMANCE TEST PROCEDURE

Performance testing of the successive approximation board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.4.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.	
Extender board 211300-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	5 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	1 reqd
Test Lead, POMONA 3782-2	1 reqd

b. Connect test setup as shown in figure 2-9 and insert extender board into position A5 in the angle encoder. Reference should also be made to figures 1-3, 1-7 and 1-21.

c. Additional instructions are given in the procedural steps.

2.3.4.2 Step-by-Step Procedure. Table 2-5 provides a step-by-step procedure for checking the performance of the successive approximation board.

Table 2-5. Successive Approximation Board P/N 206489-1 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	With power off, use DMM to check value of all resistors.			Remove and replace defective resistors as necessary.
2.	Switch on test equipment.			

Table 2-5. Successive Approximation Board P/N 206489-1 Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
3.	Using the oscilloscope, monitor UNI-CLOCK, CLOCK, SC and EC waveforms.	Edge-pins 10, 8,7 and E.	Waveforms as shown in figure 1-3.	Troubleshoot associated circuits.
4.	Move probes (except MAIN TRIG IN on edge-pin 10) to monitor U12 output and CONV DATA OUTPUTS 21^{11}, $9^{2}{}^{10}$ and 2^{9}.	U12-3. Edge-pins 5,F and L.	Output state dependent on angle input.	Troubleshoot associated circuits.
5.	Move probes (except MAIN TRIG IN on edge-pin 10) to monitor CONV DATA OUTPUTS 2^{8}_{5}, 2^{7} 2^{6}, 2^{5} waveforms.	Edge-pins 11, 12,X and 20.	Output state dependent on angle input.	Troubleshoot associated circuits.
6.	Move probes (except MAIN TRIG IN on edge-pin 10) to monitor CONV DATA OUTPUTS 2^{4}_{2}, 2^{3}_{1}, 2^{2}, 2^{1} waveforms.	Edge-pins W, 22,23, and 21.	Output state dependent on angle input.	Troubleshoot associated circuits.
7.	Switch off test equipment and disconnect test setup.			

2.3.5 ADDRESS/COMBINATION BOARD P/N 209508-1 PERFORMANCE TEST PROCEDURES

Performance testing of the address/combination board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.5.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.	
Extender board 211300-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	5 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	1 reqd
Test Lead, POMONA 3782-2	1 reqd

b. Connect test setup as shown in figure 2-10 and insert extender board into position A6 in the angle encoder (figure 2-1). Reference should also be made to figures 1-8 and 1-12.

c. Additional instructions are given in the procedural steps.

2.3.5.2 Step-by-Step Procedure. Table 2-6 provides a step-by-step procedure for checking the performance of the address/combination board.

Table 2-6. Address/Combination Board P/N 209508-1 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment and monitor $\overline{EC}$10, EC, SC and STOP CLOCK waveforms on the oscilloscope.	Edge-pins F, U and Y.	Waveforms as shown in figure 1-3.	Troubleshoot associated circuits.
2.	Disconnect probe from edge-pin F and use it to monitor the CONV COMP output.	Edge-pin 23.	Positive-going 10us pulse once every milli-second.	Troubleshoot U8 and associated circuit.

Table 2-6. Address/Combination Board P/N 209508-1
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
3.	Move probes (except MAIN TRIG IN on edge-pin 10) to monitor AZ DATA READY, EL DATA READY, AZ REG UPDATE, EL REG UPDATE waveforms.	Edge-pins AA, 25, 22 and Z.	Waveforms as shown in figure 1-3.	Troubleshoot associated circuits.
4.	Move probes (except MAIN TRIG IN on edge-pin 10) to monitor STOP CLOCK, SELECT COARSE (ELEVATION), SELECT COARSE, (AZIMUTH), SELECT FINE (ELEVATION) waveforms.	Edge-pins Y, 12, 21 and CC.	Waveforms as shown in figure 1-3.	Troubleshoot associated circuits.
5.	Move one probe to monitor SELECT FINE (AZIMUTH) waveform.	Edge-pin 20.	Waveform as shown in figure 1-3.	Troubleshoot associated
6.	Disconnect all probes.			
7.	Connect a probe from MAIN TRIG IN on the oscilloscope to edge-pin F.			
8.	Using two probes, check input and output logic levels of U18,U17,U16 and U13. Rotate 5-inch DIAL ASSEMBLY and note one-for-one change input to output.	Input/output pins as per figure 1-8.	TTL logic levels: 1=+2.4 to +5 V. 0=0 to +0.5 V.	Remove and replace defective IC.

Table 2-6. Address/Combination Board P/N 209508-1
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
9.	Repeat step 8 for U15 and U14.		As step 8.	As step 8.
10.	Switch off test equipment and disconnect test setup.			

2.3.6 DUAL OUTPUT REGISTERS BOARD P/N 212194-2, PERFORMANCE TEST PROCEDURES

Performance testing of the dual output register board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.6.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.	
Extender board 212189-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	4 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	1 reqd
Test Lead, POMONA 3782-2	1 reqd

b. Connect test setup as shown in figure 2-11 and insert extender board into position A6 in the angle encoder (figure 2-1). Reference should also be made to figures 1-3, 1-9 and 1-23.

c. Additional instructions are given in the procedural steps.

2.3.6.2 Step-by-Step Procedure. Table 2-7 provides a step-by-step procedure for checking the performance of the dual output registers board.

Table 2-7. Dual Output Registers Board P/N 212194-2 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment and monitor SELECT COARSE (AZIMUTH) SELECT COARSE (ELEVATION) and $\overline{EC}$ waveforms on the oscilloscope.	Edge-pins 11, 4, 8 and 6.	Waveforms as shown in figure 1-3.	Troubleshoot ADDRESS/ COMBINATION pcb ASSEMBLY and associated wiring.
2.	Disconnect all probes.			
3.	Using two probes, check inputs to outputs for a one to one correlation.	Input/ Output edge-pins as per figure 1-9.	TTL logic levels: 1=+2.4 to +5 V. 0=0 to +0.5 V.	Remove and replace defctive IC's as necessary. Use DMM to check resistors and resistor packs U3, U6.
4.	Switch off test equipment and disconnect test setup.			

2.3.7 ADDER/COMPLEMENTER BOARD P/N 212814-1 PERFORMANCE TEST PROCEDURES

Performance testing of the adder/complementer board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.7.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.

Extender board 212194-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	1 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	1 reqd
Test Lead, POMONA 3782-2	1 reqd

b. Connect test setup as shown in figure 2-12 and insert extender board into position A8 or A13 in the angle encoder (figure 2-1) as required. Reference should also be made to figures 1-10 and 1-24.

c. Additional instructions are given in the procedural steps.

2.3.7.2 Step-by-Step Procedure. Table 2-8 provides a step-by-step procedure for checking the performance of the adder/complementer board.

Table 2-8. Adder/Complementer Board P/N 212814-1 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment and set all OFFSET and DIRECTION switches U1 - U3 to the 'on' (closed) position.			
2.	Using the oscilloscope, check on a one to one basis that the outputs are the same as inputs.	Input/ Output edge-pins as per figure 1-10	TTL logic levels, 1=+2.4 to +5V 0=0V to +0.5V.	Remove and replace defective IC's or switches as necessary. Use DMM to check resistors.
3.	One at a time, set OFFSET switches to the 'off' (open) position and observe bit change at the output.	Input/ Output edge-pins as per figure 1-10.	TTL logic levels. 1=+2.4 to +5V 0=0V to +0.5V.	Remove and replace defective IC's or switches as necessary. Use DMM to check resistors.
4.	Set DIRECTION switch to the 'off' (open) position and check that output bits are the reverse of the input bits.	Input/ Output edge-pins as per figure 1-10.	TTL logic levels. 1=+2.4 to +5V. 0=0 to +0.5V.	Remove and replace defective IC's or switches as necessary. Use DMM to check resistors.

Table 2-8. Adder/Complementer Board P/N 212814-1
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
5.	Set 5-inch DIAL ASSEMBLY to 45^{o} and DIRECTION switch to 'on' (closed) position. Set OFFSET switches for a reading of 45^{o} on BCD DISPLAY.			
6.	Switch off test equipment and disconnect test setup.			

2.3.8 BINARY/BCD 10^{2} - 10^{-2} DECADES BOARD P/N 207730-2 AND BINARY/BCD 10^{-3} DECADE BOARD P/N 207733-3 PERFORMANCE TEST PROCEDURES

Performance testing of the binary BCD decade boards consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.8.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.
Extender board 211300-1 1 reqd
Oscilloscope, TEKTRONIX 7633-05 1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26 2 reqd
Time Base, Plug-in TEKTRONIX 7B53A 1 reqd
Probe, TEKTRONIX P6101 2 reqd
Multimeter, Digital (DMM), FLUKE 8860A 1 reqd
Test Lead, POMONA 3782-0 1 reqd
Test Lead, POMONA 3782-2 1 reqd

b. Connect test setup as shown in figure 2-13 and insert extender board into position A9,A14,A10 or A15 in the angle encoder (figure 2-1) as required. Since these boards normally operate in pairs, ensure that the 'round-off' and carry bits are accurately simulated if they are tested separately. Numeric values for each bit of each decade are given in paragraphs 1.2.8. Reference should also be made to figures 1-12, 1-13, 1-25 and 1-26.

c. Additional instructions are given in the procedural steps.

2.3.8.2 Step-by-Step Procedure. Table 2-9 provides a step-by-step procedure for checking the performance of the binary BCD decade boards.

Table 2-9. Binary BCD Decade Boards P/N 207730-2 and 207733-3 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment.			
2.	Check that the BCD DISPLAY shows the same reading as 5-inch DIAL ASSEMBLY.			a. Determine the input bit pattern required for correct reading. b. Using figure 1-12 or 1-13, check output bit pattern and troubleshoot adder and ROM matrix. Check the 'pull-up' resistors. c. Remove and replace defective components as necessary. d. One digit blank or not showing decimal character - remove and replace associated defective ROM (SN74185A).
3.	Switch off test equipment and disconnect test setup.			

2.3.9 DIFFERENTIAL LINE DRIVER BOARD P/N 212815-1 PERFORMANCE TEST PROCEDURES

Performance testing of the differential line driver board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.9.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Test setup as shown in figure 2-1.	
Extender board 212189-1	1 reqd
Oscilloscope, TEKTRONIX 7633-05	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Probe, TEKTRONIX P6101	2 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Test Lead, POMONA 3782-0	1 reqd
Test Lead, POMONA 3782-2	1 reqd

b. Connect test setup as shown in figure 2-14 and insert extender board into position A11, A12, A16 or A17 in the angle encoder (figure 2-1) as required. Reference should also be made to figures 1-14 and 1-27.

c. Additional instructions are given in the procedural steps.

2.3.9.2 Step-by-Step Procedure. Table 2-10 provides a step-by-step procedure for checking the performance of the differential line driver board.

Table 2-10. Differential Line Driver Board P/N 212815-1 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment.			
2.	Using the oscilloscope, check input and output waveforms.	Input/ output edge-pins as per figure 1-14.	TTL logic levels. 1 = +2.4 to +5 V. 0 = 0 to +0.5 V.	Remove and replace defective IC's as necessary.
3.	Switch off test equipment and disconnect test setup.			

2.3.10 1200 HZ OSCILLATOR BOARD P/N 211190-5 PERFORMANCE TEST PROCEDURES

Performance testing of the 1200 Hz oscillator board consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.10.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment :

Test setup as shown in figure 2-1.	
Extender Board 211300-1.	1 reqd
Oscilloscope TEKTRONIX 7633-05	1 reqd
Vertical Amplifier, TEKTRONIX 7A13	1 reqd
Dual Trace, Plug-in TEKTRONIX 7A26.	1 reqd
Time Base, Plug-in, TEKTRONIX 7B53A.	1 reqd
Probe TEKTRONIX P6101	4 reqd
Multimeter, Digital (DMM), FLUKE 8860A	1 reqd
Decade, Resistor, 1434G	1 reqd
Counter, Electronic, 5345A-01	1 reqd
Test Lead, POMONA 3782-36-0	3 reqd
Test Lead, POMONA 3782-36-2	3 reqd
Test Lead, POMONA 3782-C-36	1 reqd

b. Connect test setup as shown in figure 2-15 and insert extender board into position A18 in the angle encoder (figure 2-1). Reference should also be made to figures 1-15 and 1-28.

c. Additional instructions are given in the procedural steps.

2.3.10.2 Step-by-Step Procedure. Table 2-11 provides a step-by-step procedure for checking the performance of the 1200 Hz oscillator board.

Table 2-11. 1200 Hz Oscillator Board P/N 211190-5
Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Switch on test equipment.			
2.	Observe waveform shown on the oscilloscope vertical amplifier plug-in and note reading on electronic counter.	Edge-pins 20/X and 21/Y.	1200 Hz ± 20% sine wave (approx) 34 V p-p (ampl).	Troubleshoot U1 and associated circuit if basic oscillator is working. (Refer to step 3).

Table 2-11. 1200 Hz Oscillator Power Supply Board P/N 211190-5 (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
3.	Observe waveform on CHA and CHB on the oscilloscope dual trace plug-in. circuit.	Edge-pins 8/J and 5/E.	Equal sine waves of 1200 Hz ±5% (approx) 10 V p-p in ±5. (ampl).	Troubleshoot basic oscillator (U2, U3) and associated circuits. Use DMM and decade resistor to select value of SAT resistors. NOTE Select R11 for frequency as close as possible to 1200 Hz and R3 for amplitude as close as possible to 10 V p-p. R11 and R3 are slightly interactive.
4.	Switch off test equipment and disconnect test setup.			

2.3.11 EXTENDER BOARD (80-WAY) P/N 212189-1 AND EXTENDER BOARD (50-WAY) P/N 211300-1, PERFORMANCE TEST PROCEDURES

Performance testing of the extender boards consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.11.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps.

a. Obtain the following test equipment:

Multimeter, AVO Model 8.

b. Remove relevant extender board from the angle encoder and place on a clean bench surface.

c. Additional instructions are given in the procedural steps.

2.3.11.2 Step-by-Step Procedure. Table 2-12 provides a step-by-step procedure for checking the performance of the extender board.

Table 2-12. Extender Boards P/N 212189-1 and P/N 211300-1 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Using the AVO Model 8 set to OHMS ÷ 100 range, check the continuity of each track including the edge-connector contacts.		Meter reading less than 0.5 ohm.	No continuity. a. Inspect track for breaks and repair if necessary. b. Troubleshoot edge-connector. Remove and replace if necessary. High or unstable meter reading. a. Re-make any soldered joint. b. Troubleshoot edge-connector. Remove and replace if necessary.
2.	Using the AVO Model 8 set to OHMS x 100 range check the insulation between adjacent tracks.		Meter reading greater than 50 M ohms.	Low meter reading. a. Check board for score marks and scratches. Clean and re-varnish board as necessary. b. Troubleshoot edge-connector. Remove and replace if necessary.

2.3.12 ±15 V POWER SUPPLY ASSEMBLY R115 PERFORMANCE TEST PROCEDURES

Performance testing of the ±15 V power supply assembly consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.12.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following test equipment:

Transformer SUPERIOR ELECTRIC 216B	1 reqd
Oscilloscope TEKTRONIX 7633-05	1 reqd
Vertical Amplifier, TEKTRONIX A713	1 reqd
Probe TEKTRONIX P6101	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Multimeter, Digital FLUKE 8860A	1 reqd
Multimeter, AV08	1 reqd
Load, Electronic EL-750B	1 reqd
Test Lead POMONA B-48-0	2 reqd
Test Lead POMONA B-48-2	2 reqd
Test Lead POMONA 1370-48-0	2 reqd
Test Lead POMONA 3170-48-2	2 reqd
Test Lead POMONA 1370-48-0	2 reqd
Test Lead POMONA 1370-48-2	2 reqd
Adaptor POMONA 3744	6 reqd
Power Cable Pacific Electrocord C2114-03M-GY	1 reqd

b. On transformer 216B, set the output voltage for 110 Vac. Switch all power supplies OFF.

c. On the load electronic, set the current control adjustment fully ccw (minimum current).

d. Set the AV08 to read 300 Vac.

e. Connect test equipment as shown in figure 2-17. Reference should also be made to figures 1-16 and 1-31.

f. Additional instructions are given in the step-by-step procedure.

CAUTION

Do not connect the ground lead on the power cable C2114-03M-GY

2.3.12.2 Step-by-Step Procedure. Table 2-13 provides a step-by-step procedure for checking the performance of the power supply assembly R115.

Table 2-13. Power Supply Assembly R115
Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Set the transformer power supply ON/OFF switch to ON.			
2.	Connect DMM set to read +50 Vdc, as detailed.	+V (+ve), -V (-ve).	30 ± 0.1 Vdc.	For no output, check S1, T1, D1-D4 and associated components. For reduced or excessive output, continue step-by-step procedures.
3.	Remove DMM and connect as detailed.	+V (+ve), COM (-ve).	+15 ± 0.1 Vdc.	Adjust P1 to obtain performance standard. If fault not cleared, check A1, Q2, Q1 and associated components.
4.	Remove DMM and connect as detailed.	-V (+ve), COM (-ve).	-15 ± 0.1 Vdc.	Adjust P2 to obtain performance standard. If fault not cleared, check A2, Q5, Q7, Q6 and associated components.
5.	On the electronic load, adjust the current control for 0.75 A.			

Table 2-13. Power Supply Assembly R115
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
6.	Observe DMM	-V (+ve), COM (-ve).	-15 Vdc ± 2 mV.	Check Q8 and associated components.
7.	Remove DMM and connect as detailed.	+V (+ve), COM (-ve).	+15 Vdc ± 2mV.	Check Q3 and associated components
8.	Remove DMM and using oscilloscope check ripple content as detailed.	+V (+ve), -V (-ve).	Less than 25 mV p-p.	Check C1, C2, C8 and C9.
9.	Observe AV08 and increase transformer output to 130 Vac.			
10.	Repeat steps 2 to 8 (DO NOT ADJUST LOAD ELECTRONIC).	As steps 2 to 8.	As steps 2 to 8.	As steps 2 to 8.
11.	Set power supplies to off and remove test equipment.			

2.3.13 ±5 V POWER SUPPLY ASSEMBLY 210 PERFORMANCE TEST PROCEDURES

Performance testing of the ±5 V power supply assembly consists of preliminary and step-by-step procedures. The preliminary procedures identify the test equipment required and provide instructions for making the required test setup and connections. The step-by-step procedure checks the performance of the unit and identifies possible causes of a malfunction.

2.3.13.1 Preliminary Procedures. Prior to performing the step-by-step procedure, perform the following steps:

a. Obtain the following equipment:

Transformer SUPERIOR ELECTRIC 216B	1 reqd
Oscilloscope TEKTRONIX 7633-05	1 reqd
Vertical Amplifier, TEKTRONIX A713	1 reqd
Probe TEKTRONIX P6101	2 reqd
Time Base, Plug-in TEKTRONIX 7B53A	1 reqd
Multimeter, Digital FLUKE 8860A	1 reqd
Multimeter, AVO8	1 reqd
Load, Electronic EL-750B	1 reqd
Test Lead POMONA B-48-0	2 reqd
Test Lead POMONA B-48-2	2 reqd
Test Lead POMONA 1370-48-0	2 reqd
Test Lead POMONA 1370-48-2	2 reqd
Adaptor POMONA 3744	6 reqd
Power Cable Pacific Eletrocord 62114-03M-GY	1 reqd

b. On transformer 216B, set the output voltage for 110 Vac. Switch all power supplies OFF.

c. On the load electronic, set the current control adjustment fully ccw (minimum current).

d. Set the AVO8 to read 300 Vac.

e. Connect test equipment as shown in figure 2-18. Reference should also be made to figures 1-17 and 1-32.

f. Additional instructions are given in the step-by-step procedure.

CAUTION

Do not connect the ground lead on the power cable C2114-03M-GY

2.3.13.2 Step-by-Step Procedure. Table 2-14 provides a step-by-step procedure for checking the performance of the power supply assembly 210.

Table 2-14. Power Supply Assembly 210 Performance Test Procedure

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
1.	Connect the DMM set to read +200 Vdc, as detailed.	D1, D3 junction (+ve), GND (-ve).	+180 Vdc ± 10%.	Check L6, L7 D1-D4 and associated components.

Table 2-14. Power Supply Assembly 210
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
2.	Connect oscilloscope, set to measure 20 kHz, as detailed.	T1-1 (CHAN 1), T1-3 (CHAN 2).	Two 20 kHz waveforms, approximately squarewave, 180° out of phase.	Check Q1, Q2 Q3 and associated components.
3.	Connect the DMM, set to read +30 Vdc, as detailed.	Q2 emitter (+ve), GND (-ve).	+22 ± 0.5 Vdc.	Check Q4, Q5, D6, D7, T2 and associated components.
4.	Connect the DMM set to read +10 Vdc, as detailed and note exact reading.	+V (+ve), -V (-ve).	+5 ± 0.05 Vdc.	If DMM reads +6.9 ± 0.1 Vdc, check Q8-Q10 and associated components. If output is zero, check Q6, Q7 and associated components.
5.	Adjust STATIC CURRENT control on the electronic load for 10 A load current.			
6.	Repeat step 4.	As step 4.	Voltage difference less than 5 mV from step 4.	Check L1, D15, P3 and associated components.
7.	Connect the oscilloscope as detailed and check check output voltage ripple content.	+V (CHAN 1)	Less than 25 mVp-p.	Check C9, C10, C18 and associated components.

Table 2-14. Power Supply Assembly 210
Performance Test Procedure (Continued)

Step	Procedure	Test Point	Performance Standard	If Indication Abnormal
8.	Increase the output of transformer 216B to 130 Vac ± 2% and repeat steps 1 to 7 inclusive.			
9.	Switch off all power supplies and disconnect all test equipment.			

2.4 RESISTANCE MEASUREMENTS

Resistance measurements on each LRU of the angle encoder are made only to check suspected faulty components and are contained in the relevant performance test procedure.

2.5 VOLTAGE AND WAVEFORM MEASUREMENTS

All necessary voltage and waveform measurements on the LRU's of angle encoder are contained in the relevant performance test procedure.

PART 2

SECTION II

DISASSEMBLY AND REASSEMBLY

2.6 GENERAL

This section describes the disassembly and reassembly of the LRU's contained within the angle encoder unit.

2.7 DISASSEMBLY

Disassembly of each LRU, where applicable, is described in detail in the following paragraphs.

2.7.1 CIRCUIT BOARD ASSEMBLIES

Remove defective components/items using standard workshop practice and observing standard safety precautions.

CAUTION

Ensure correct precautions are taken when handling CMOS logic elements.

2.7.2 ±15 V POWER SUPPLY ASSEMBLY-R115

To gain access to internal components, proceed as follows:

a. Remove the two screws from the side of the power supply where the power output leads are located.

b. Remove the three screws from the opposite side of the power supply.

c. Remove the ventilated top cover to expose the power supply circuitry.

d. Remove the two screws securing the wires to the filter capacitor terminals. Tag and remove the wires.

e. Remove the two mounting screws at the base of the filter capacitor, and remove the capacitor.

f. Remove the three screws securing the circuit board to the capacitor.

g. Disconnect and tag the wires from the circuit board.

2.7.3 +5 V POWER SUPPLY ASSEMBLY-210

To gain access to internal components, proceed as follows:

a. Remove the two screws from the side of the power supply where the power output leads are located.

b. Remove the three screws from the opposite side of the power supply.

c. Remove the ventilated top cover to expose the power supply circuitry.

d. Remove the two screws securing the wires to the filter capacitor terminals. Tag and remove the wires.

e. Remove the two mounting screws at the base of the filter capacitor, and remove the capacitor.

f. Remove the three screws securing the circuit board to the capacitor.

g. Disconnect and tag the wires from the circuit board.

2.8 REASSEMBLY

To reassemble an LRU, proceed as described in the following paragraphs.

2.8.1 CIRCUIT BOARD ASSEMBLIES

Replace components/items using standard workshop practice and observing standard safety precautions.

CAUTION

Ensure correct precautions are taken when handling CMOS logic elements.

2.8.2 ± 15 V POWER SUPPLY ASSEMBLY-R115

Reverse the procedure given in paragraph 2.7.2.

2.8.3 +5 V POWER SUPPLY ASSEMBLY-210

Reverse the procedure given in paragraph 2.7.3.

PART 2

SECTION III

REPAIR

2.9 GENERAL

This section provides instructions for performing depot repair, lubrication (if applicable) and periodic maintenance of the LRU's in the angle encoder unit.

2.10 REPAIR

Special cleaning, painting, repair or other processing procedures are not required for the circuit boards or the power supplies. Repair consists of removing and replacing the defective component/item using standard workshop practice.

WARNING

Turn off all power supplies before carrying out any cleaning or repair procedures. When using solvents, provide adequate ventilation and avoid breathing hazardous fumes. When cleaning with compressed air, wear safety goggles and use clean dry air at a pressure not exceeding 20 N/cm^2 (25 lb/in^2).

CAUTION

Never use ethyl alchohol or methyl ethyl ketone as a cleaning solvent as these substances dissolve printed circuit boards and connectors.

2.11 LUBRICATION

Not applicable.

2.12 PERIODIC MAINTENANCE

Not applicable.

PART 2

SECTION IV

ALIGNMENT AND ADJUSTMENT

2.13 GENERAL

This section describes the offsite alignment and adjustment procedures which can be performed on the LRU's in the angle encoder unit.

2.14 ALIGNMENT AND ADJUSTMENT

The following paragraphs contain adjustment procedures for the +5 V power supply (210) and the ±15 V power supply (R115). Test equipment and connections are detailed in the step-by-step procedures.

2.14.1 ± 15 V POWER SUPPLY ASSEMBLY-R115 OUTPUT VOLTAGE ADJUSTMENT.

To adjust the output voltage, proceed as follows:

a. Ensure that the angle encoder is switched off.

b. Connect digital voltmeter 8030A-01 across the power supply output (HI to +S terminal and LO to -S terminal) using patch cords POMONA 1370-48-2 and POMONA 1370-48-0 respectively.

c. Switch on angle encoder and adjust VOL ADJ preset control to obtain a reading of +30 ± 0.3 V.

d. Switch off the angle encoder and disconnect the test equipment.

e. If the reading cannot be obtained, carry out the performance test detailed in part 2, section I, sub-paragraph 2.3.12.

2.14.2 +5 V POWER SUPPLY ASSEMBLY-210 OUTPUT VOLTAGE ADJUSTMENT.

To adjust the output voltage, proceed as follows:

a. Ensure that the angle encoder is switched off.

b. Connect digital voltmeter 8030A-01 across the power supply output (HI to +S terminal and LO to -S terminal) using patch cords POMONA 1370-48-2 and POMONA 1370-48-0 respectively.

c. Switch on the angle encoder and adjust VOL ADJ preset control to obtain a reading of +5 V ± 0.1 V.

d. Switch off the angle encoder and disconnect the test equipment.

PART 2

SECTION V

CALIBRATION

2.15 GENERAL

This section describes the offsite calibration procedures which can be performed on the LRU's in the angle encoder unit.

2.16 CALIBRATION

The following paragraphs contains step-by-step calibration procedures to be carried out after the removal and replacement of a defective component/item on an LRU. Test equipment and connections are detailed in the steps and supported, where necessary, by diagrams included at the end of this part.

2.16.1 SIGNAL CONDITIONING BOARD P/N 206497-13 CALIBRATION

Reference should be made to figures 1-3, 1-19, 2-1 and 2-19. Proceed as follows:

a. Connect standard test setup as shown in figure 2-1 and ensure that the angle encoder is switched off.

b. Disconnect input cable from 10:1 transducer 801681-4.

c. Remove the synchronous demodulator/multiplexer boards and on each board connect patch cords (POMONA 3781-12-9) as shown in figure 2-19. (This effectively short-circuits edge-pins CC to BB, T to S, P to H and 5 to E to give zero inputs).

d. Replace the synchronous demodulator/multiplexer boards.

e. Remove the address/combination board and connect a patch cord (POMONA 3787-C-36) to U6 as shown in figure 2-19.

f. Replace the address/combination board and connect the patch cord to TRIGGER IN terminal on the oscilloscope. (This triggers the oscilloscope from the start-of-conversion signal SC OUT).

g. Set oscilloscope VERTICAL SENSITIVITY control to 5 millivolt/division.

h. Extend the board under calibration by means of the 50-way extender board and switch on all equipment.

i. Using a probe (TEKTRONIX P6028), connect CH1 of the oscilloscope to edge-pin K and adjust preset potentiometer R36 for a level of 0 $\pm$ 0.001 V.

j. Move probe to edge-pin M (or 11) and adjust preset potentiometer R47 for a level of 0 ± 0.001 V.

k. Move probe to edge-pin J and adjust preset potentiometer R15 for a level of 0 ± 0.001 V.

l. Move probe to edge-pin R (or 14) and adjust preset potentiometer R26 for a level of 0 ± 0.001 V.

m. Switch off and remove all test equipment and test connections.

2.16.2 SIN/COS NETWORK BOARD P/N 206499-1 CALIBRATION

Reference should be made to figures 1-6, 1-20 and 2-1.

Proceed as follows:

a. Connect standard test setup as shown in figure 2-1 and ensure that the angle encoder is switched off.

b. Extend the sin/cos network board by means of the 50-way extender board (A20) and switch on all equipment.

c. Set 5-inch dial assembly to exactly 45°. (i.e., SIN dc = COS dc).

d. Using an oscilloscope and a suitable probe, monitor the 2^{10}X input on edge-pin 17.

e. Adjust offset potentiometer R31 to the position where the 2^{10}X input just changes from logic 0 (0V to +0.5 V) to logic 1 (+2.4 V to +5 V).

f. Switch off all equipment.

2.17 SELECT-AT-TEST PROCEDURES

Select-at-test procedures, where applicable, are included in the performance tests for each LRU.

PART 2

SECTION VI

POSTREPAIR CHECKOUT

2.18 GENERAL

This section contains the postrepair checkout procedures for the LRU's in the Angle Encoder Unit.

2.19 POSTREPAIR CHECKOUT

Postrepair checkout is performed to verify that the repaired LRU meets the minimum specification requirements.

2.19.1 SYNCHRONOUS DEMODULATOR/MULTIPLEXER BOARD P/N 212195-6 POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.1.

2.19.2 SIGNAL CONDITIONING BOARD P/N 206497-13, POSTREPAIR CHECKOUT

Carry out peformance test (or relevant part of performance test) as described in paragraph 2.3.2.

2.19.3 SIN/COS NETWORK BOARD P/N 206499-1, POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.3.

2.19.4 SUCCESSIVE APPROXIMATION BOARD P/N 206498-1, POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.4.

2.19.5 ADDRESS/COMBINATION BOARD P/N 209508-1, POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.5.

2.19.6 DUAL OUTPUT REGISTERS BOARD P/N 212194-2, POSTREPAIR CHECKOUT

Carry out peformance test (or relevant part of performance test) as described in paragraph 2.3.6.

2.19.7 ADDER/COMPLEMENTER BOARD P/N 212814-1, POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.7.

2.19.8 BINARY/BCD 10^{2} - 10^{-2} DECADES BOARD P/N 207730-2 AND BINARY/BCD 10^{-3} DECADE BOARD (A10, A15), POSTREPAIR CHECKOUT.

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.8.

2.19.9 DIFFERENTIAL LINE DRIVER BOARD, P/N 212815-1 POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.9.

2.19.10 1200 HZ OSCILLATOR BOARD P/N 211190-5 POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.10.

2.19.11 EXTENDER BOARD, 80-WAY P/N 212189-1 AND EXTENDER BOARD, 50-WAY P/N 211300-1 POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.11.

2.19.12 15 V POWER SUPPLY ASSEMBLY-R115 POSTREPAIR CHECKOUT.

Carry out peformance test (or relevant part of performance test) as described in paragraph 2.3.12.

2.19.13 +5 V POWER SUPPLY ASSEMBLY-210 POSTREPAIR CHECKOUT

Carry out performance test (or relevant part of performance test) as described in paragraph 2.3.13.

PART 2

MAINTENANCE AND REPAIR

SECTION VII

PACKAGING/PACKING FOR RESHIPMENT

2.20 GENERAL

This section describes the unpacking, or packing and packaging for reshipment of the angle encoder unit LRUs.

2.21 UNPACKAGING

To unpack the angle encoder unit LRU from its shipping container, proceed as follows, taking care that the equipment is not dropped or handled carelessly:

a. Remove the nailed down top of the plywood-sheathed shipping crate.

b. Lift the corrugated container from the shipping crate and place it on the assigned work area.

c. Open the corrugated container and remove the inner cardboard carton, usually sealed in a moisture/vapour-proof carrier bag.

d. Untape and remove the carrier bag from around the inner cardboard carton.

e. Cut open the inner cardboard carton, remove sufficient cushioning material, and extract the LRU, taking care not to damage it.

f. Visually inspect the assembly and report any damage to the appropriate stores authority.

2.22 REUSABLE CONTAINERS

Do not destroy the shipping container and packing or materials as they can be used for reshipment.

2.23 PACKAGING/PACKING FOR RESHIPMENT

To repack an LRU for reshipment, reverse the procedure detailed in paragraph 2.21, using adhesive tape to seal the cardboard carton and the moisture/vapour proof bag.

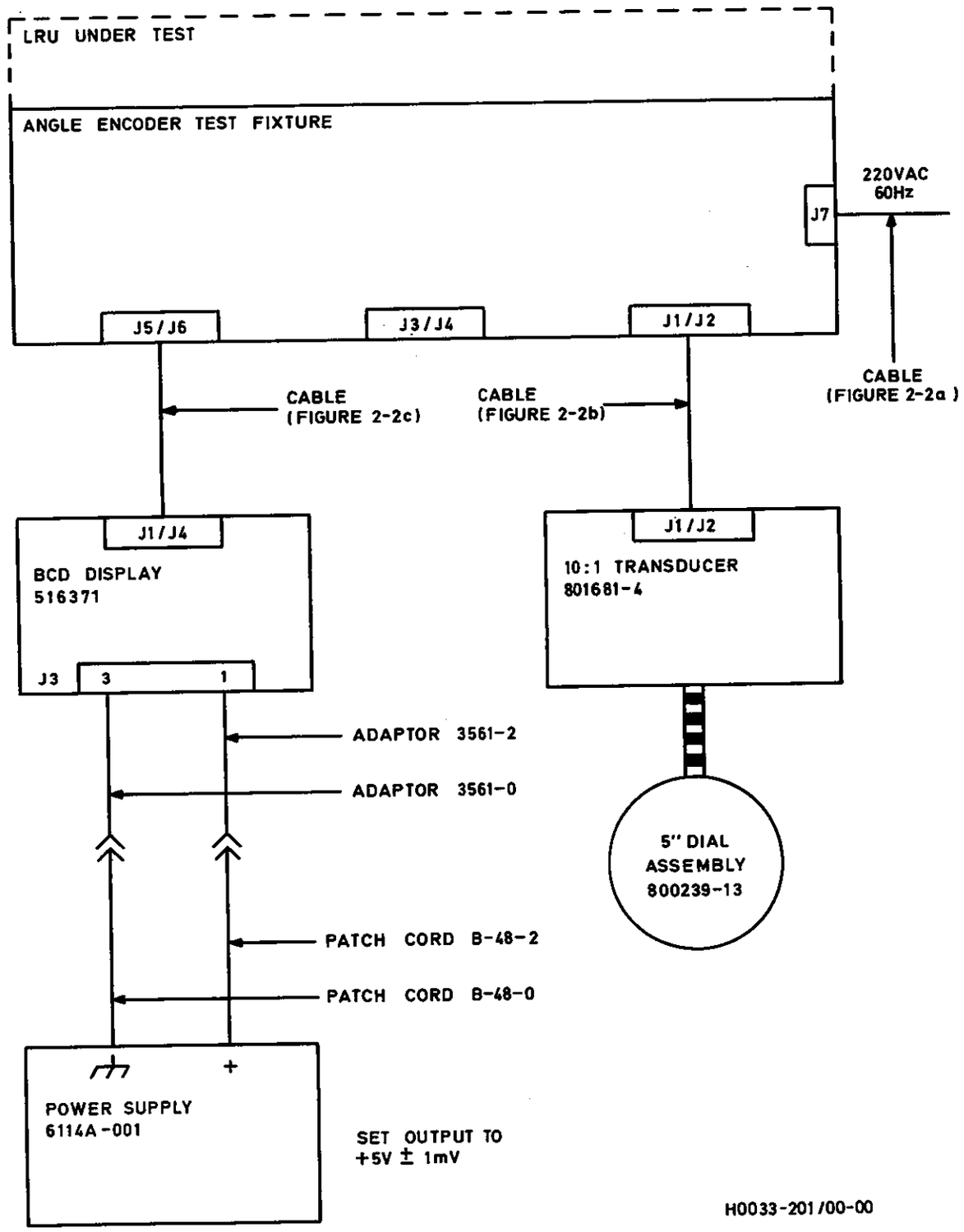


Figure 2-1. Standard Test Setup : Interconnection Diagram

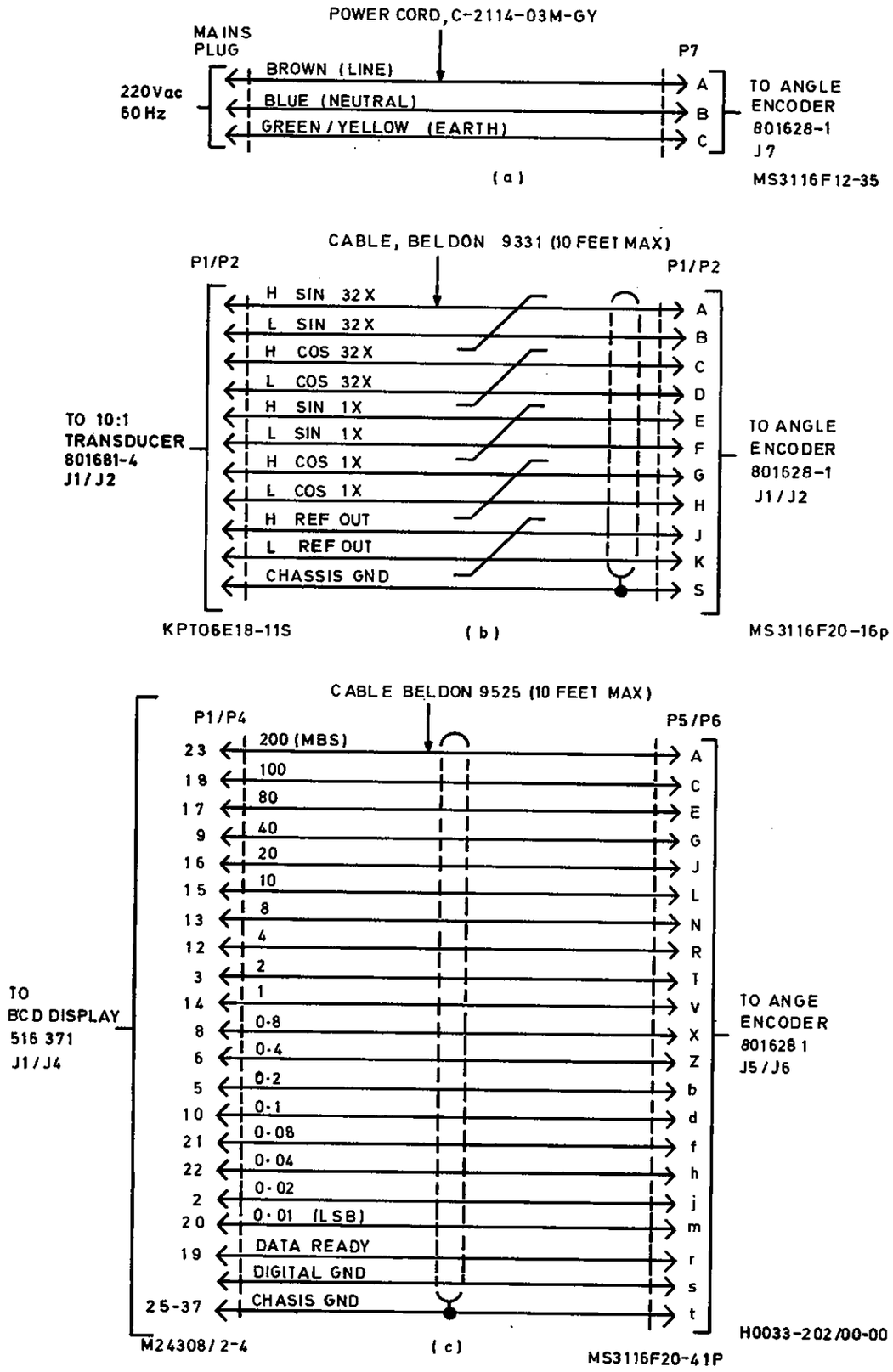


Figure 2-2. Standard Test Setup : Special-to-Type Cables

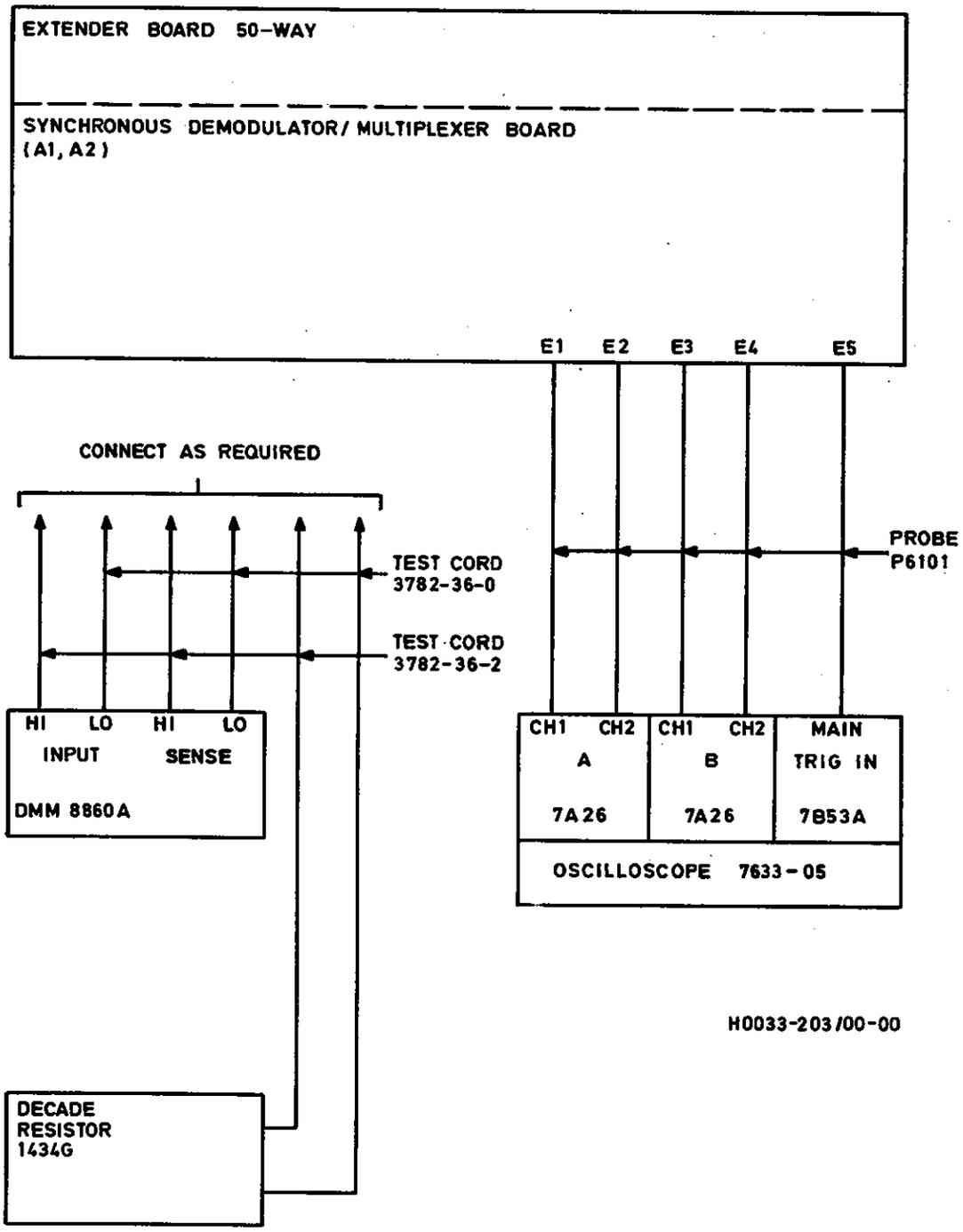


Figure 2-3. Synchronous Demodulator/Multiplexer Board : Test Setup Diagram

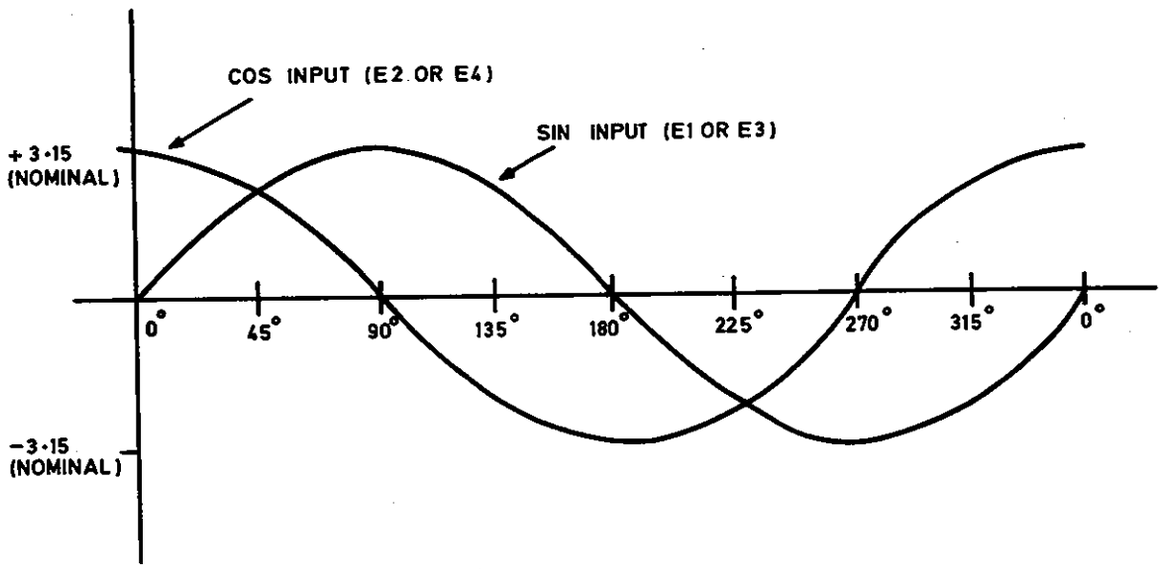
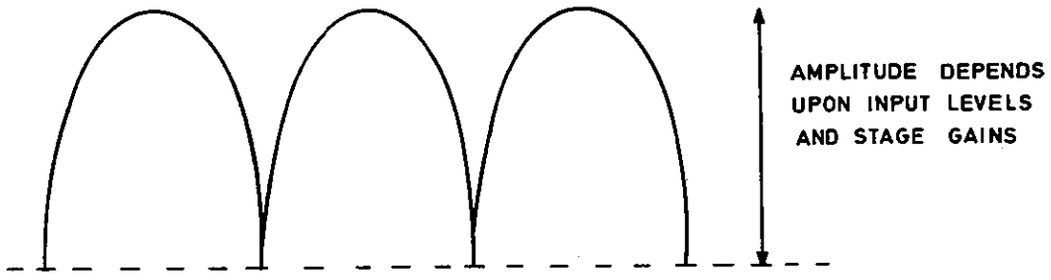
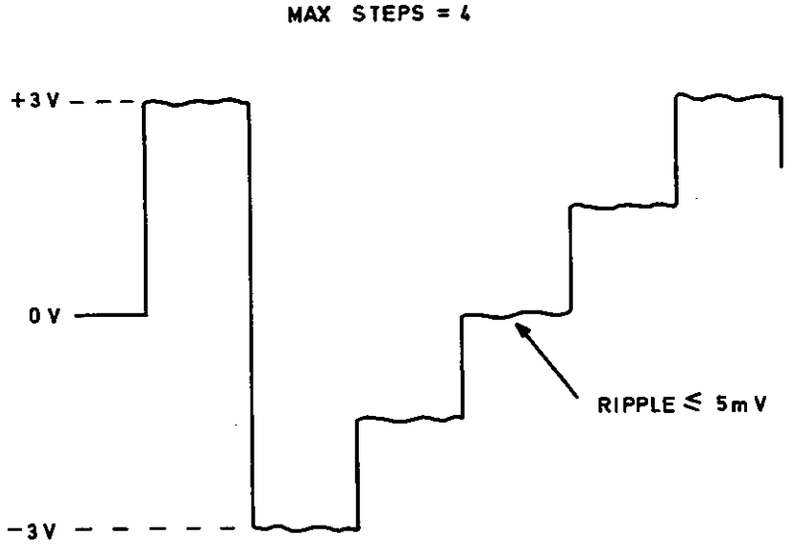


Figure 2-4. Synchronous Demodulator/Multiplexer Board : SIN/COS Phase Relationship



(a)



(b)

H0033-205/00-00

Figure 2-5. Synchronous Demodulator/Multiplexer Board : Typical Waveforms

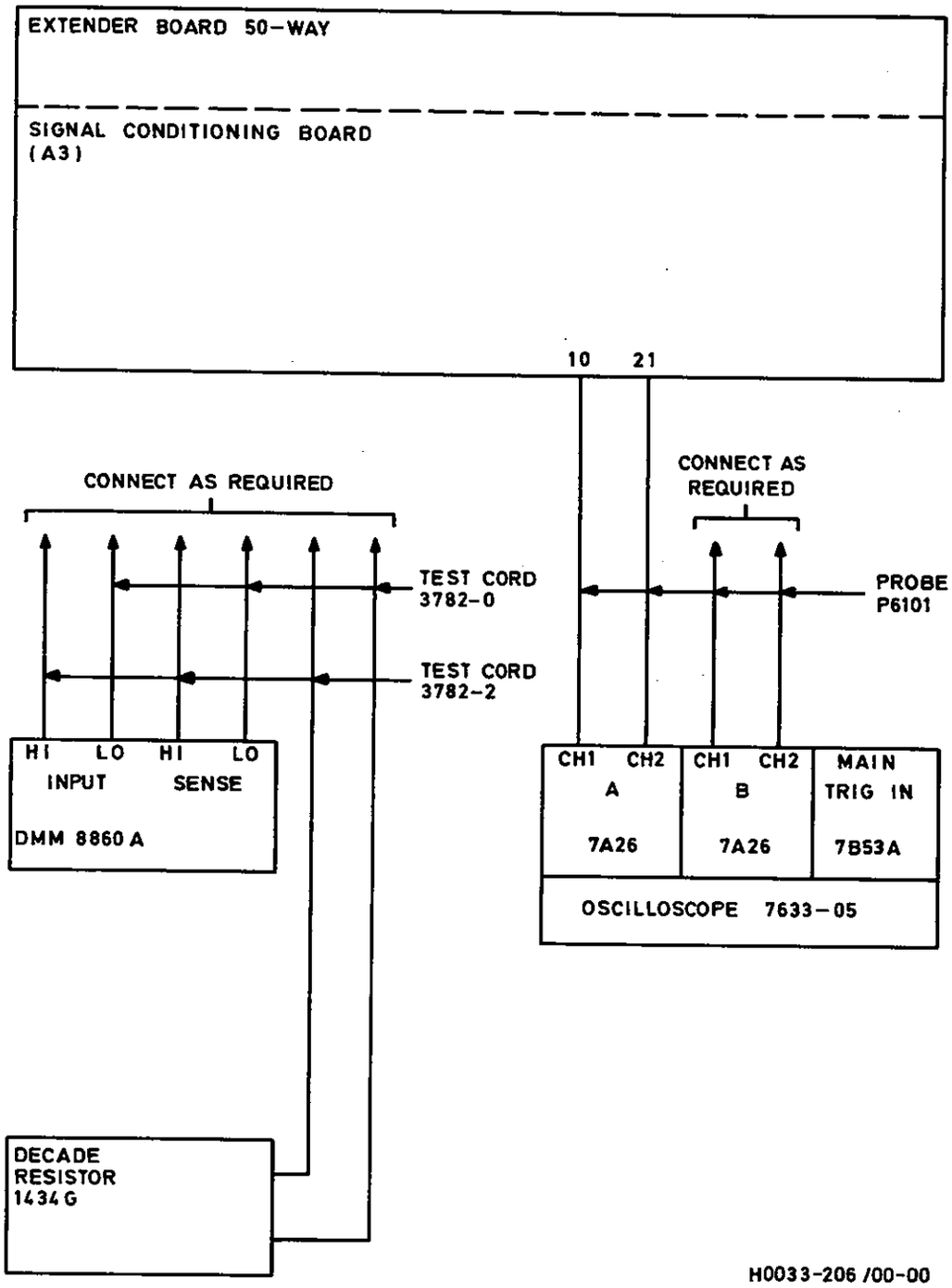


Figure 2-6. Signal Conditioning Board: Test Setup Diagram

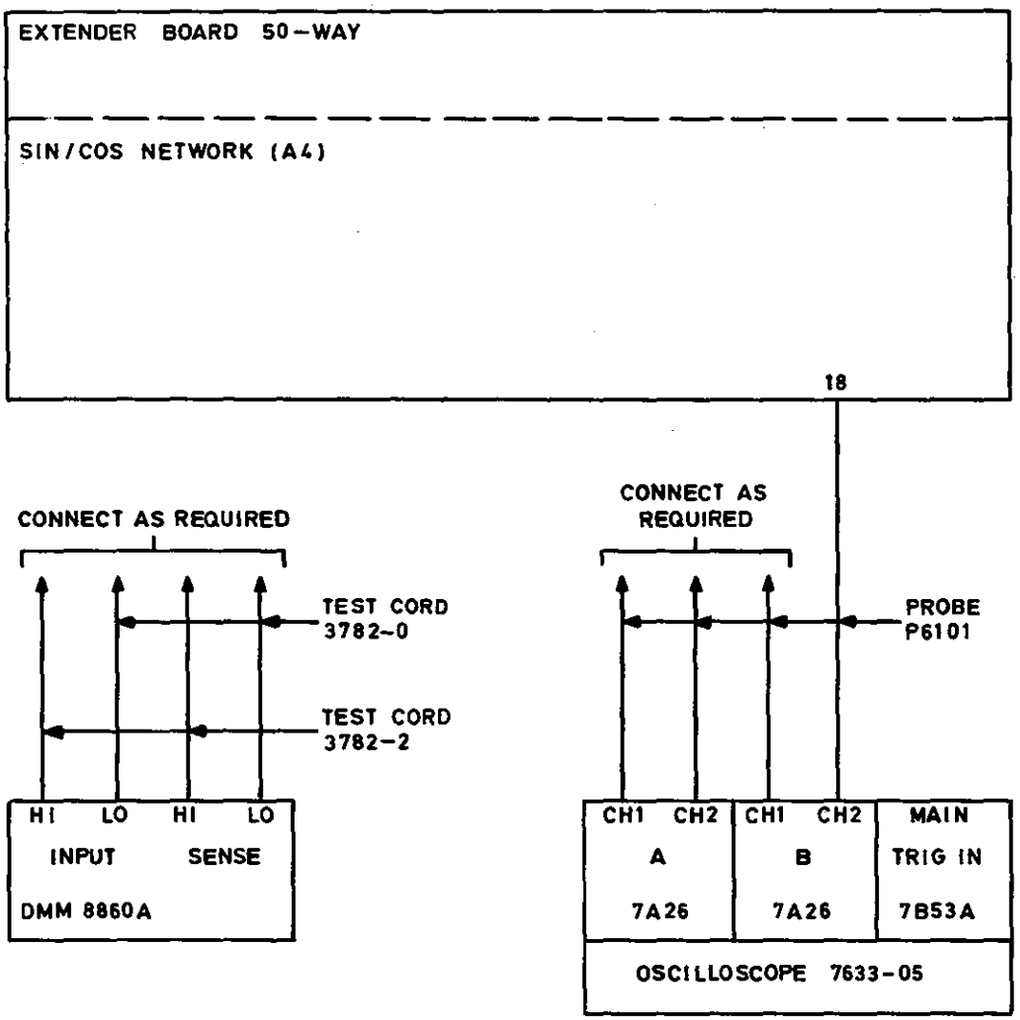


Figure 2-7. SIN/COS Network Board : Test Setup Diagram

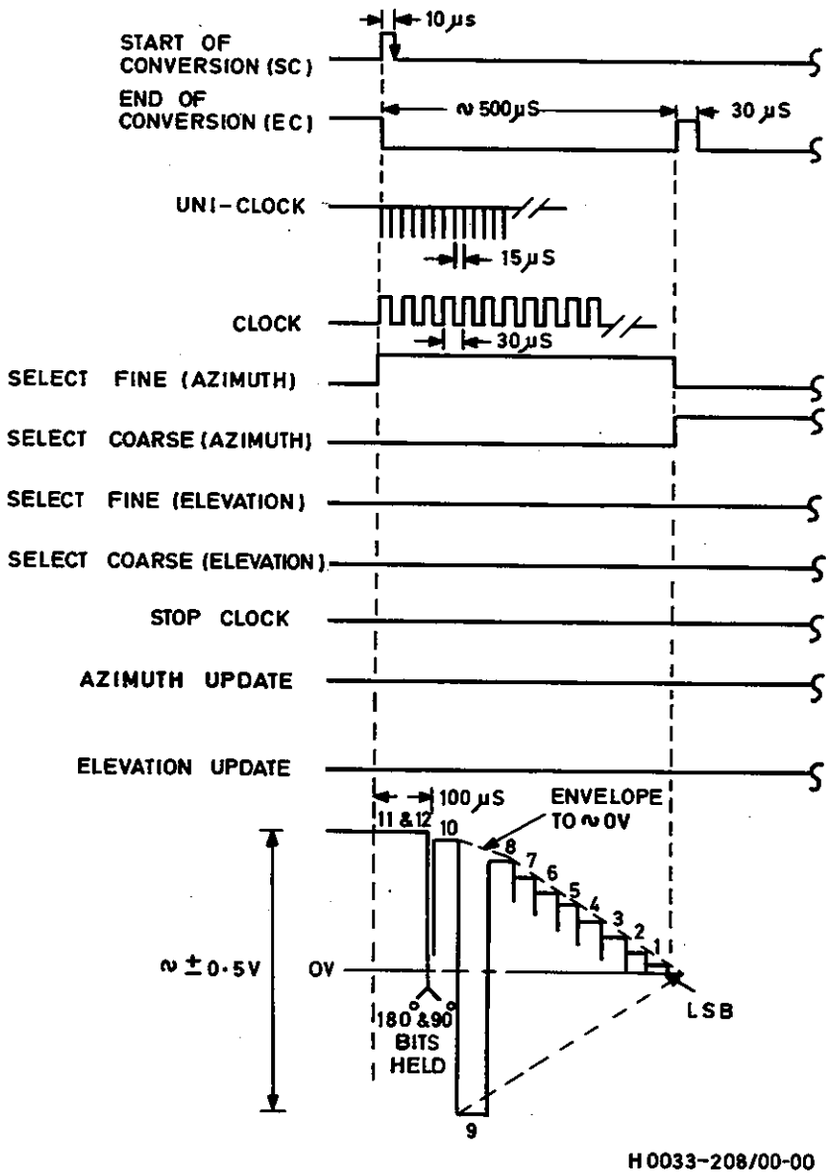


Figure 2-8. Sin/Cos Network : Typical Output Waveform

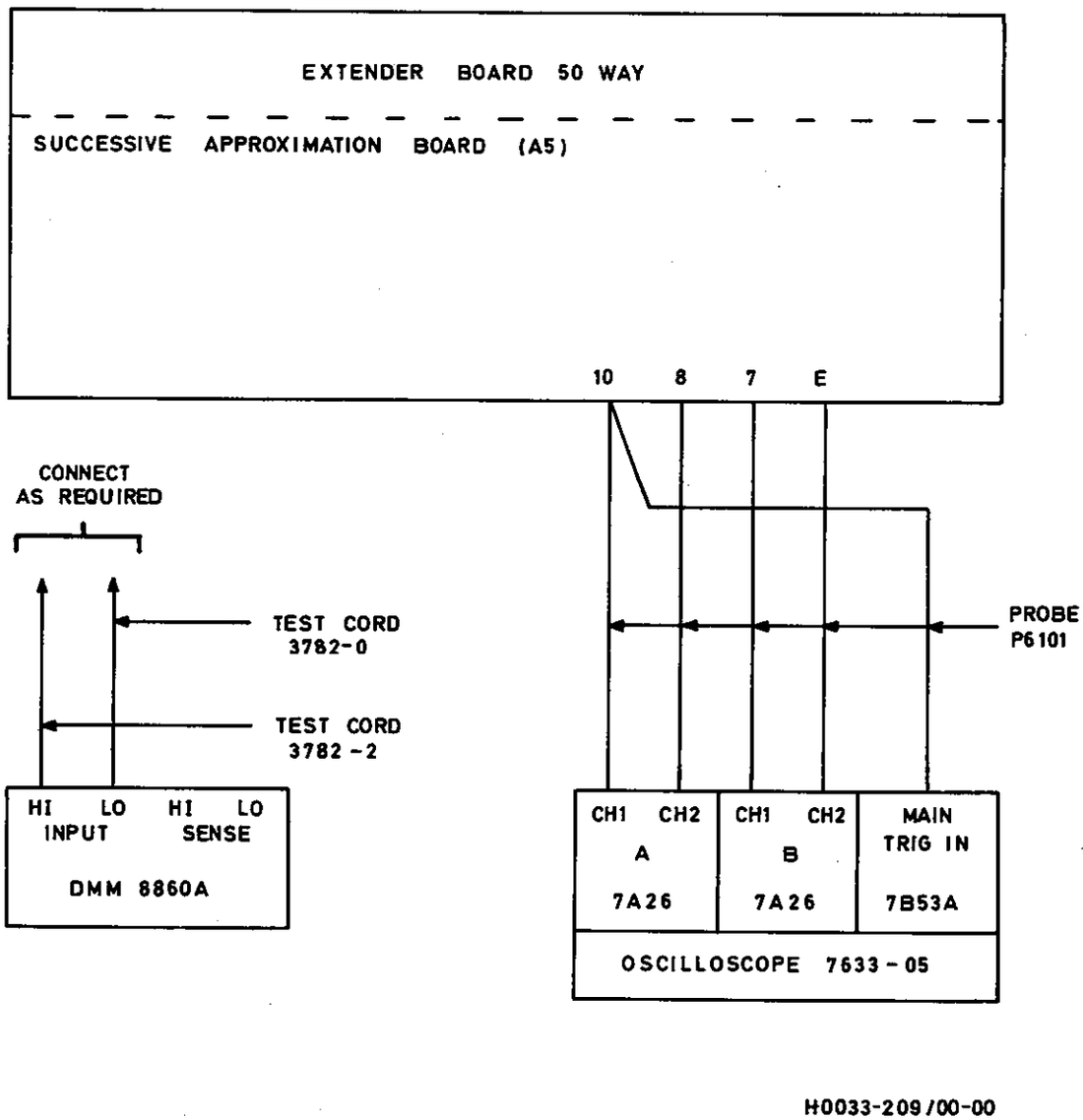


Figure 2-9. Successive Approximation Board : Test Setup Diagram

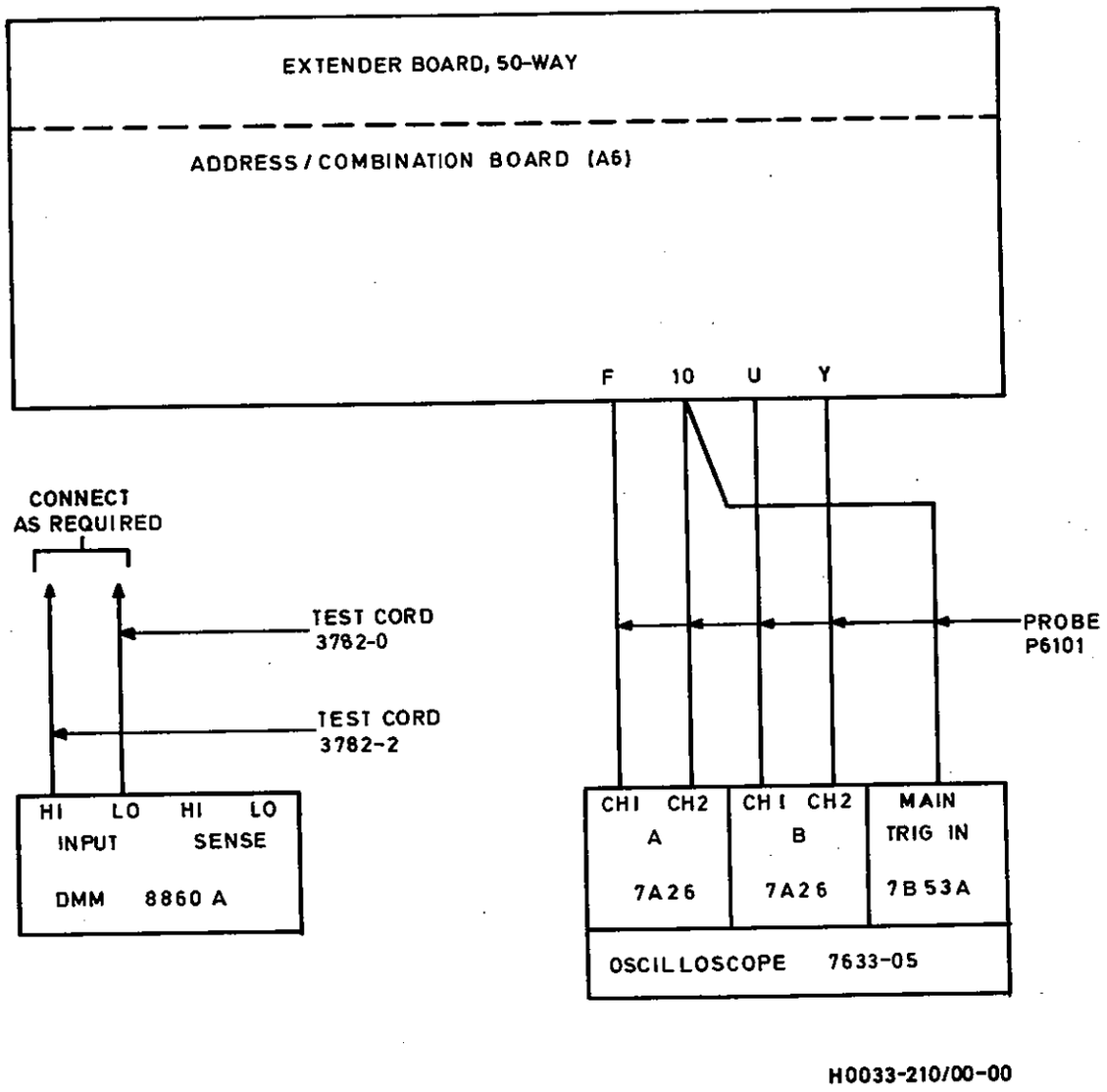


Figure 2-10. Address/ Combination Board : Test Setup Diagram

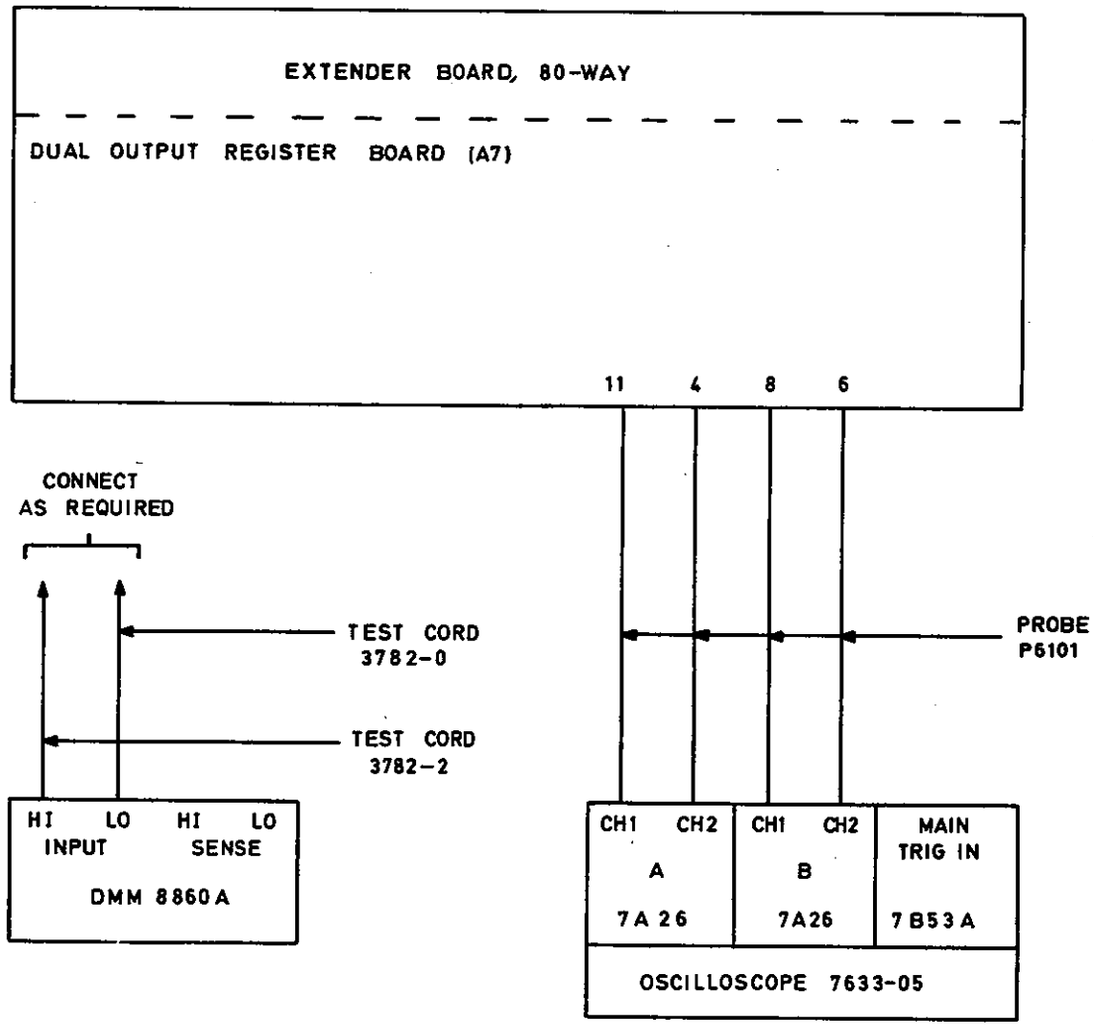


Figure 2-11. Dual Output Register Board : Test Setup Diagram

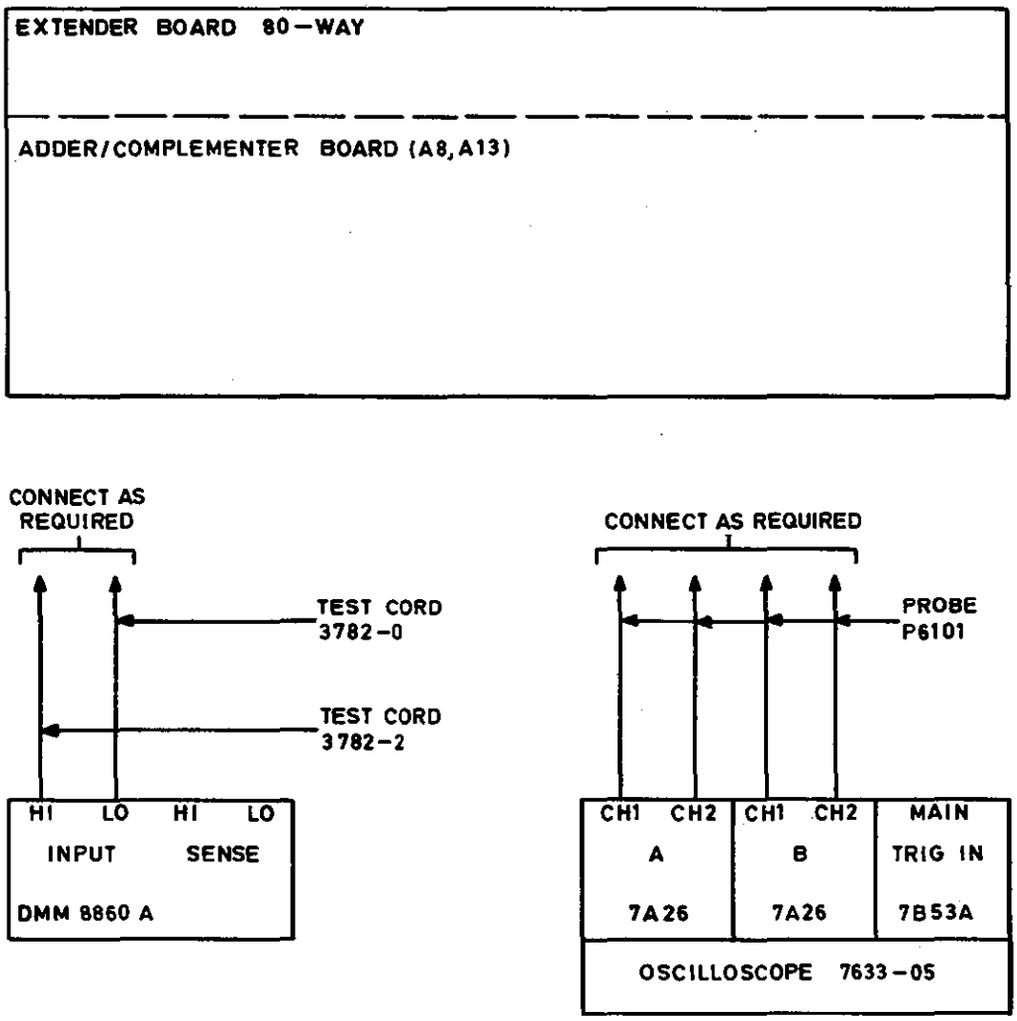


Figure 2-12. Adder/Complementer Board : Test Setup Diagram

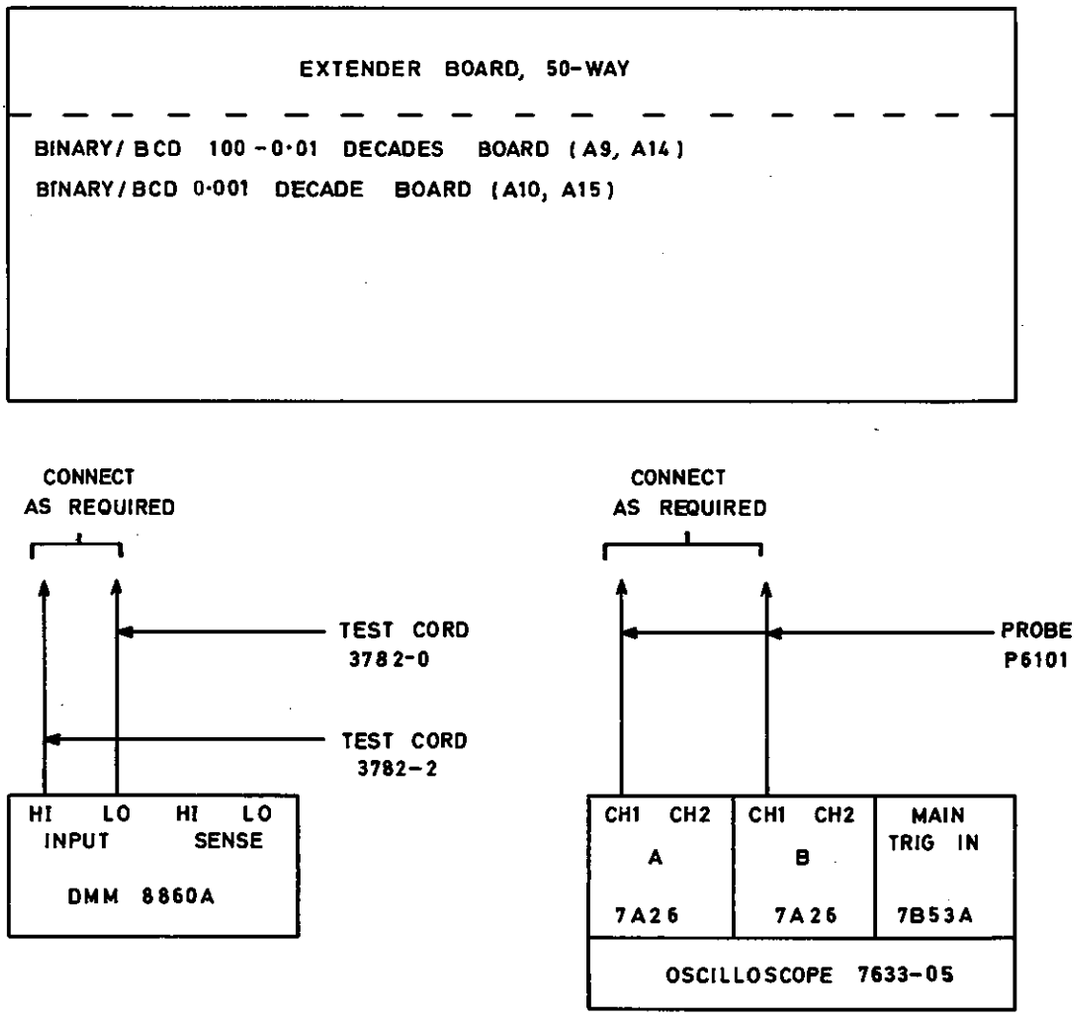


Figure 2-13. Binary/BCD 10^{2}-10^{-2} Decades Board and Binary/BCD 10^{-3} Decade Board : Test Setup Diagram

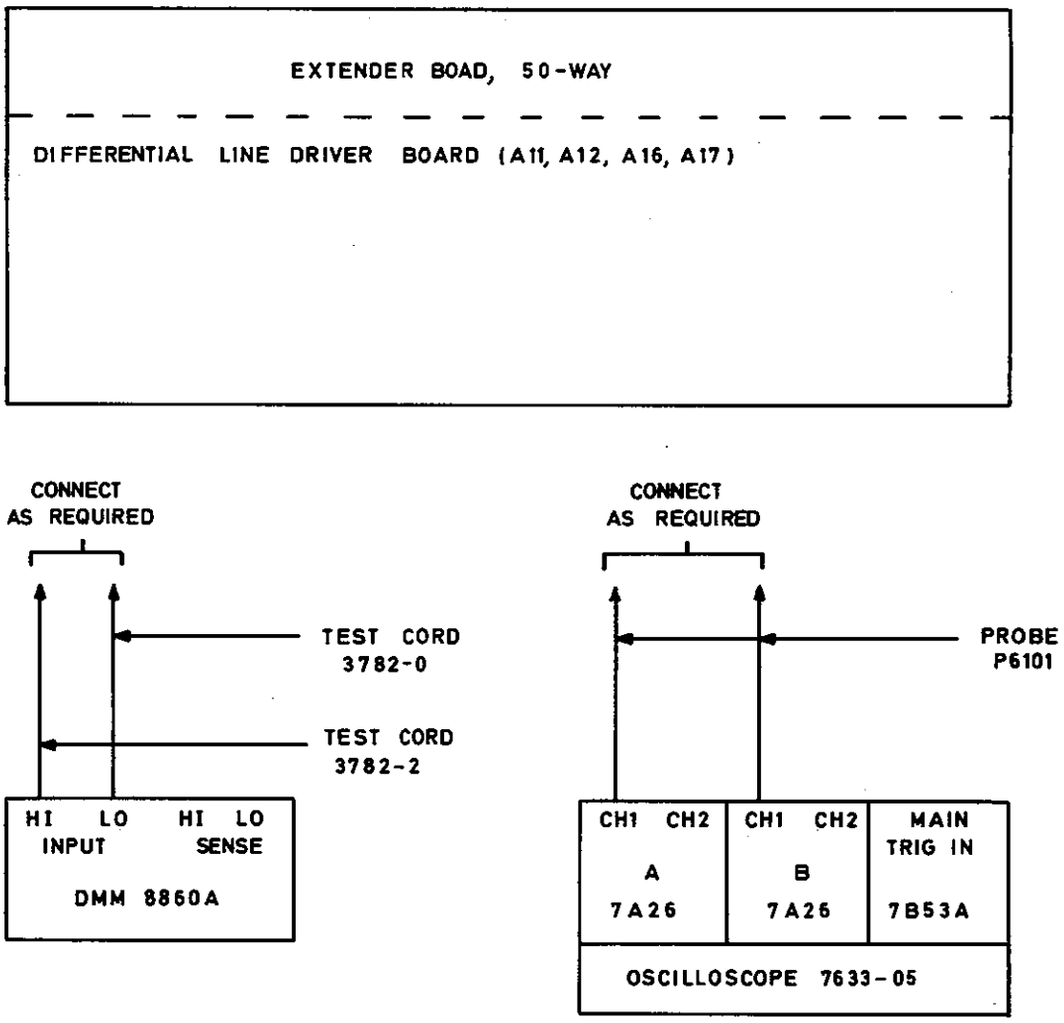
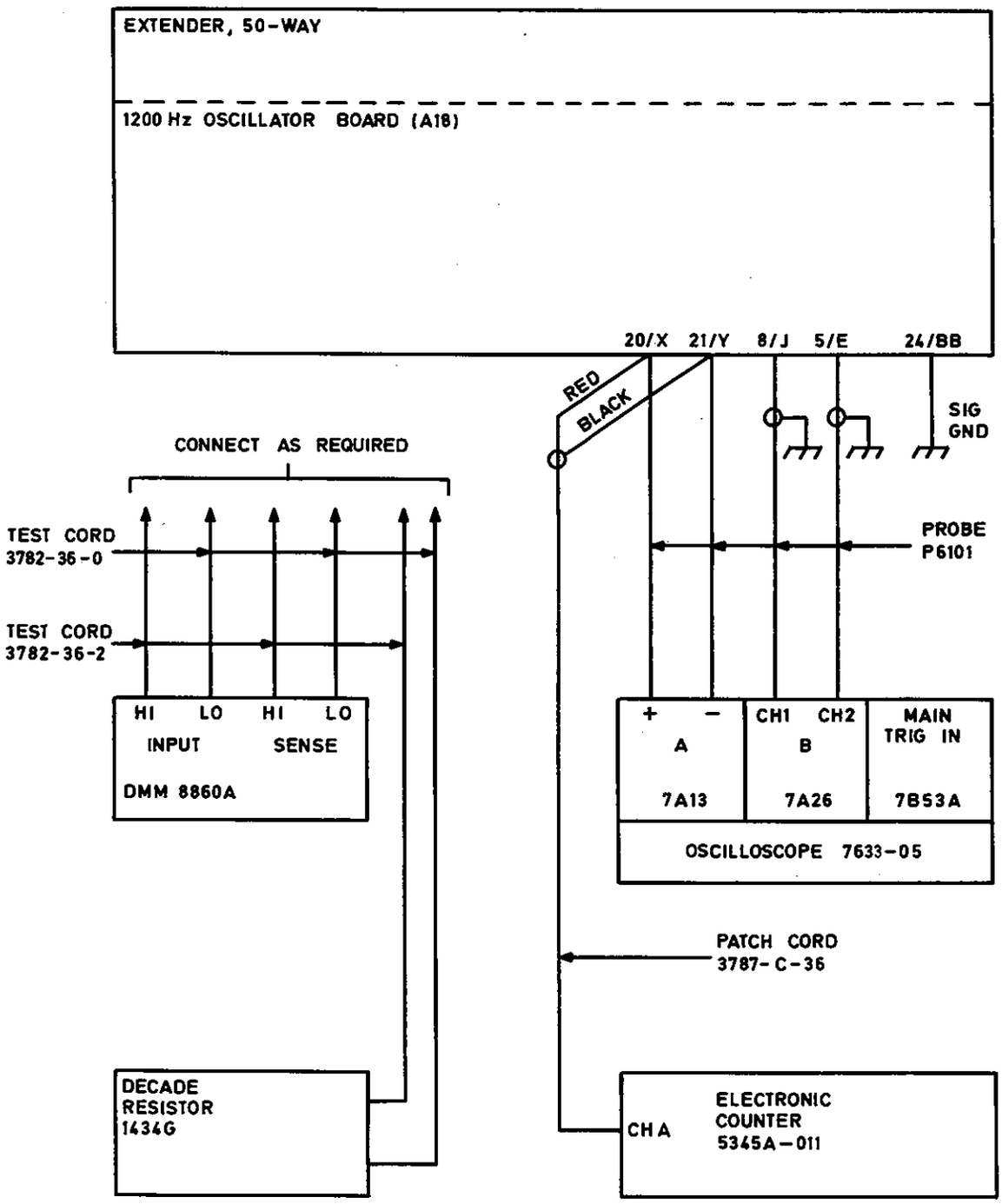
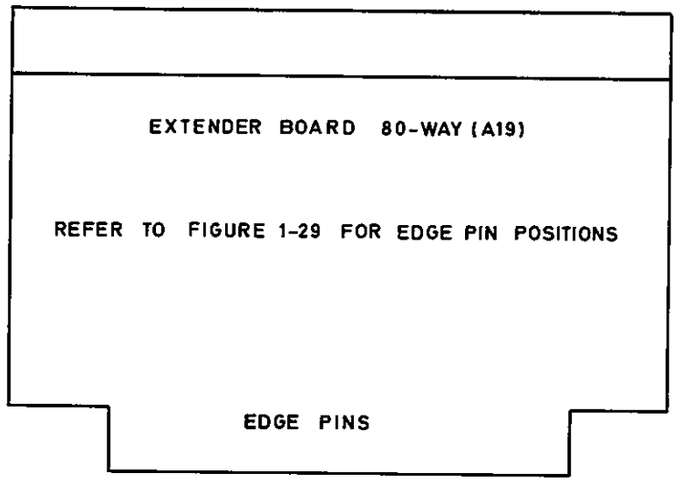


Figure 2-14. Differential Line Driver Board : Test Setup Diagram

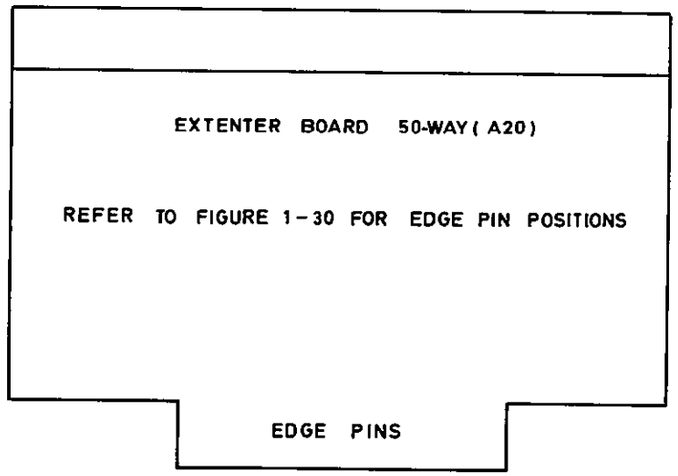


H0033-215/00-00

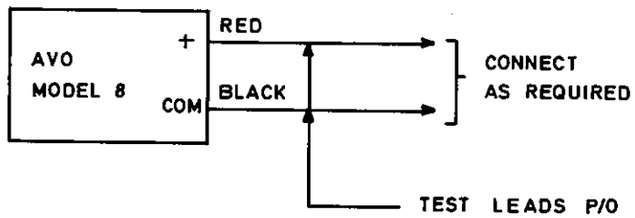
Figure 2-15. 1200 Hz Oscillator Board : Test Set-up Diagram



(a)

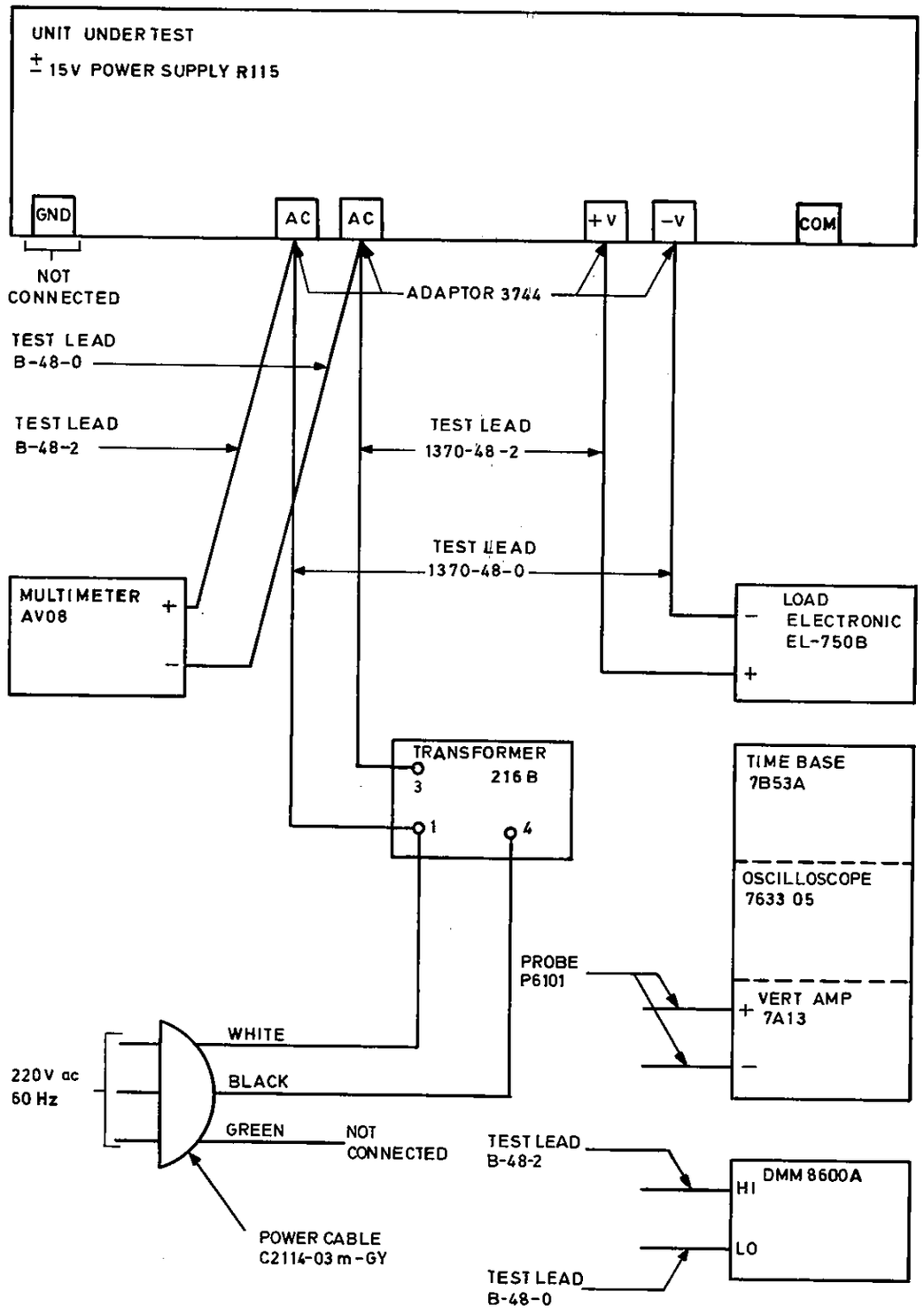


(b)



H0033-216/00-00

Figure 2-16. Extender Board 80-way and Extender Board 50-way : Test Set-up Diagram



H0033-217/00-00

Figure 2-17. ± 15 V Power Supply Assembly R115 : Test Setup Diagram

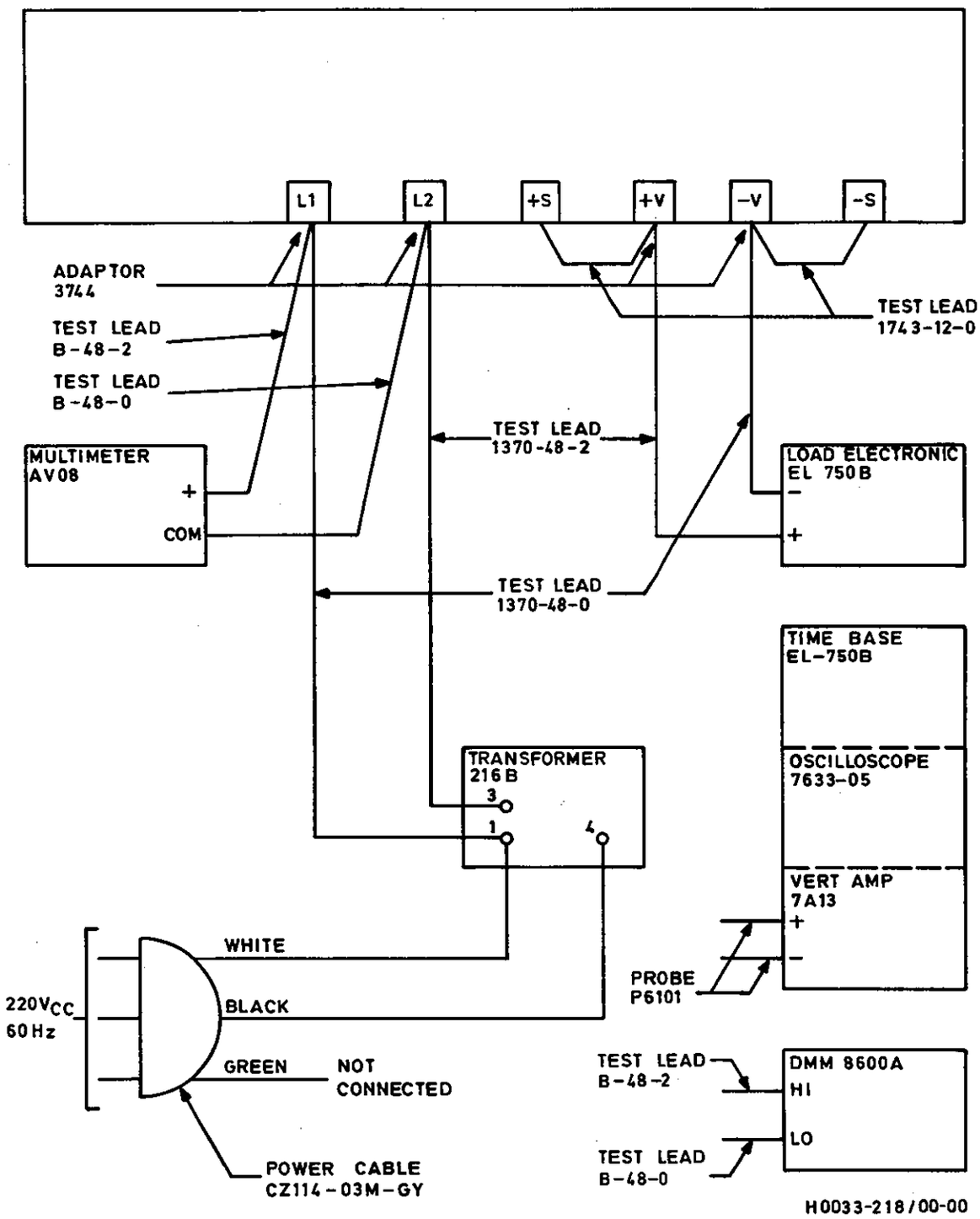


Figure 2-18. +5 V Power Supply Assembly 210 : Test Setup Diagram

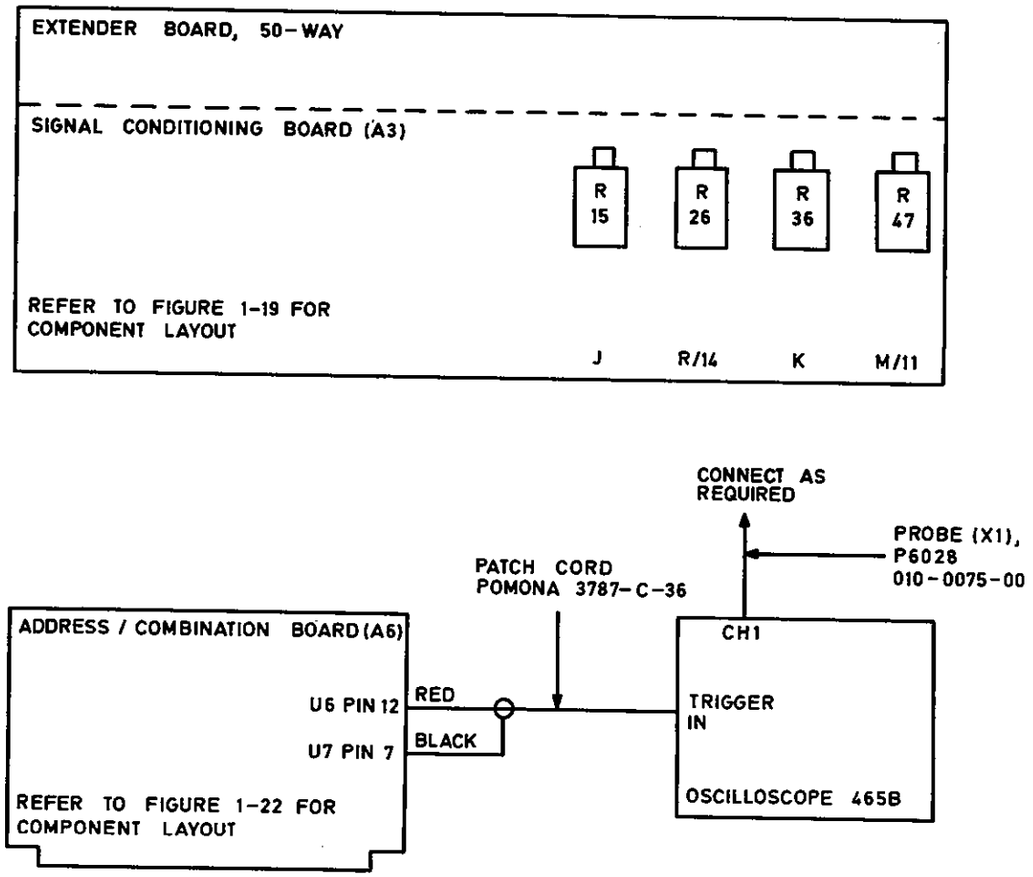


Figure 2-19. Signal Conditioning Board : Calibration Setup Diagram

PART 3

COMPONENT LIST

TABLE OF CONTENTS

LIST OF TABLES

PART 3

COMPONENT LIST

3.1 GENERAL

Part 3 consists of table 3-1, which lists the components within the angle encoder unit. For each component, the list specifies circuit reference designator, description, value, rating, tolerance, federal manufacturer's code, part number, and NATO stock number.

Table 3-1. Component List

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
	ANGLE CONVERTER,ANT				14742	801628-1	
	KEY,POLARIZING				71785	50-PK-2	
A8J1,A11J1-A13J1, A16J1,A17J1	CONNECTOR,RCPT,ELEC				71785	50-80C-10 A16J1,A17J1	
	SCREW,MACH,PNH,XREC	4-40X7/16			96906	MS51957-16	
	ISOLATION KIT,VRIS				03508	A7811055	
A1,2	CKT CD ASSY,SYNC	DEMOD/MUX			14742	212195-6	
U11,14	IC,ANALOG SWITCH				34371	HI2-0200-2	
U9	IC,OPNL AMPL				27014	LM118H	
U1-8,10,12,13,15	IC,OPNL AMPL				02735	CA741T	
Q2,4,6,8	TRANSISTOR,NPN	400 MW	TO-46		80131	2N5066	
Q1,3,5,7	TRANSISTOR,PNP	400 MU	TO-46		80131	2N3677	
Q10	TRANSISTOR,SIL,NPN	75 V	.5 W		81349	JAN2N2222A	
Q9	TRANSISTOR,PNP	400 MW	TO-18		81349	JAN2N2907A	
CR1,2	SEMICOND DVC,DIODE	10 mA	75 V		80131	1N4148	
R1,2,5,7-9,11,14, 15,16,18,21-23,25, 28,62,66,69,73	RESISTOR,FXD,WW	10K OHMS	1/8 W	1/100	14742	MPC010000-01 15,16,18,21-23,25, 28,62,66,69,7	
R17,19,24,26	RESISTOR,FXD,WW	13K OHMS	1/8 W	1/100	14742	MPC013000-01	
R33,40,47,54	RESISTOR,FXD,CMPSN	5.1K OHMS	1/8 W	5 %	81349	RCR05G512JS	
R36,37,43,44,50,51, 57,58	RESISTOR,FXD,CMPSN	15K OHMS	1/8 W	5 %	81349	RCR05G153JS 57,58	
R29,30	RESISTOR,FXD,CMPSN	22K OHMS	1/8 W	5 %	81349	RCR05G223JS	
R31,32	RESISTOR,FXD,CMPSN	100 OHMS	1/8 W	5 %	81349	RCR05G101JS	
R63,71	RESISTOR,FXD,CMPSN	10K OHMS	1/8 W	5 %	81349	RCR05G103JS	
C1	CAP,FXD,CERAMIC	0.01 μF	100 V	10 %	81349	CK05BX103K	

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3-2

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
C2-5	CAP,FXD,POLYCARB	0.47 μF	50 V	10 %	84411	X463UW4749.5W2	
	CAP,FXD,POLYCARB	0.47 μF	50 V	10 %	84411	X463UW4749.5W2	
C6,7	CAP,FXD,CERAMIC	0.1 μF	100 V	10 %	81349	CK05BX104K	
C8,C9	CAP,FXD,CERAMIC	1 μF	50 V	10 %	81349	CK06BX105K	
E1-10	TERMINAL,PIN				86577	1D3-8B	
Q1-10	TRANSIPAD				13103	7717-16-DAP	
U1-10,12,13,15	TRANSIPAD				07047	10285-N	
U11,14	TRANSIPAD				07047	10462-DAP	
A3	CKT CD ASSY,SIG CONDITIONING				14742	206497-13	
A4,7	IC,OPNL AMPL,LINEAR				27014	LM709H	
A2,5	IC,OPNL AMPL				01295	SN52741L	
A3,6	IC,OPNL AMPL				18324	LM101AH	
Q11,12,16,17,18	TRANSISTOR,SIL,PNP	60 V	60 V		80131	2N2907A	
Q5,7,10,13,19	TRANSISTOR,SIL,NPN	75 V	.5 W		81349	JAN2N2222A	
Q8,9,14,15	TRANSISTOR,FET,SIL		1.8 W		80131	2N3972	
Q6	TRANSISTOR,UNJ,SIL	50 mA	0.36 W	TO-72	80131	2N3980	
CR3-8	SEMICOND DVC,DIODE	10 mA	75 V		80131	1N4148	
R15,26,36,47	RESISTOR,VAR,NONWW	10K OHMS	1 W	5 %	32997	3290H-1-103	
	RESISTOR,FXD,CMPSN	22K OHMS	1/4 W	5 %	81349	RCR07G223JS	
	RESISTOR,FXD,CMPSN	24K OHMS	1/4 W	5 %	81349	RCR07G243JS	
	RESISTOR,FXD,CMPSN	27K OHMS	1/4 W	5 %	81349	RCR07G273JS	
R10	RESISTOR,FXD,CMPSN	30K OHMS	1/4 W	5 %	81349	RCR07G303JS	
	RESISTOR,FXD,CMPSN	33K OHMS	1/4 W	5 %	81349	RCR07G333JS	
	RESISTOR,FXD,CMPSN	36K OHMS	1/4 W	5 %	81349	RCR07G363JS	
	RESISTOR,FXD,CMPSN	39K OHMS	1/4 W	5 %	81349	RCR07G393JS	
R25,46	RESISTOR,FXD,CMPSN	15 OHMS	1/4 W	5 %	81349	RCR07G153JS	
R18,39	RESISTOR,FXD,CMPSN	5.1K OHMS	1/4 W	5 %	81349	RCR07G512JS	
R19,40	RESISTOR,FXD,CMPSN	8.2K OHMS	1/4 W	5 %	81349	RCR07G822JS	
R9	RESISTOR,FXD,CMPSN	220 OHMS	1/4 W	5 %	81349	RCR07G221JS	
	RESISTOR,FXD,CMPSN	56 OHMS	1/4 W	5 %	81349	RCR07G560JS	
	RESISTOR,FXD,CMPSN	62 OHMS	1/4 W	5 %	81349	RCR07G620JS	
	RESISTOR,FXD,CMPSN	68 OHMS	1/4 W	5 %	81349	RCR07G680JS	
	RESISTOR,FXD,CMPSN	75 OHMS	1/4 W	5 %	81349	RCR07G750JS	
R12	RESISTOR,FXD,CMPSN	82 OHMS	1/4 W	5 %	81349	RCR07G820JS	
	RESISTOR,FXD,CMPSN	91 OHMS	1/4 W	5 %	81349	RCR07G910JS	
	RESISTOR,FXD,CMPSN	100 OHMS	1/4 W	5 %	81349	RCR07G101JS	
	RESISTOR,FXD,CMPSN	110 OHMS	1/4 W	5 %	81349	RCR07G111JS	

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
R11,27,34,35,48,55,	RESISTOR,FXD,CMPSN	10K OHMS	1/4 W	5 %	81349	RCR07G103JS	
56						56	
R17,38	RESISTOR,FXD,CMPSN	5.1MEG OHMS	1/4 W	5 %	81349	RCR07G515JS	
R24,45	RESISTOR,FXD,CMPSN	22K OHMS	1/4 W	5 %	81349	RCR07G223JS	
R28,49	RESISTOR,FXD,CMPSN	47K OHMS	1/4 W	5 %	81349	RCR07G473JS	
R23,44	RESISTOR,FXD,CMPSN	220K OHMS	1/4 W	5 %	81349	RCR07G224JS	
R33,54	RESISTOR,FXD,CMPSN	10 OHMS	1/4 W	5 %	81349	RCR07G100JS	
R16,37	RESISTOR,FXD,CMPSN	10MEG OHMS	1/4 W	5 %	81349	RCR07G106JS	
R13	RESISTOR,FXD,CMPSN	1K OHMS	1/4 W	5 %	81349	RCR07G102JS	
R57,58	RESISTOR,FXD,CMPSN	10MEG OHMS	1/8 W	5 %	81349	RCR05G106JS	
R20,41	RESISTOR,FXD,CMPSN	470 OHMS	1/2 W	5 %	81349	RCR20G471JS	
R21,22,42,43	RESISTOR,FXD,WW	10K OHMS	1/8 W	1/100	14742	MPC010000-01	
C9,14	CAP,FXD,CERAMIC	220 pF	50 V	25 %	93958	SC-220	
C8,13	CAP,FXD,CERAMIC	5 pF	50 V	25 %	93958	SC-5	
C7,12	CAP,FXD,CERAMIC	10 pF	50 V	25 %	93958	SC-10	
C6,11	CAP,FXD,CERAMIC	33 pF	50 V	25 %	93958	SC-33	
C5	CAP,FXD,CERAMIC	0.1 μF	200 V	10 %	81349	CK05BX331K	
	TRANSIPAD				13103	7717-16-DAP	
A4	CKT CD ASSY,SIN/COSNETWORK				14742	206499-1	
A1	IC,OPNL AMPL,LINEAR				01295	SN52709L	
Q1-3,8-11,25-36	TRANSISTOR,SIL,NPN	75 V	.5 W		81349	JAN2N2222A	
Q50-61	TRANSISTOR,PNP	400 MW	TO-18		81349	JAN2N2907A	
Q37-49	TRANSISTOR,PNP	400 MU	TO-46		80131	2N3677	
Q4-7,12-24	TRANSISTOR,NPN	400 MW	TO-46		80131	2N5066	
CR1,2	SEMICOND DVC,DIODE	10 mA	75 V		80131	1N4148	
R32	RESISTOR,FXD,CMPSN	3K OHMS	1/8 W	5 %	81349	RCR05G302JS	
R33	RESISTOR,FXD,CMPSN	10MEG OHMS	1/8 W	5 %	81349	RCR05G106JS	
R17,20,24,27,30,53,	RESISTOR,FXD,CMPSN	6.8 OHMS	1/8 W	5 %	81349	RCR05G682JS	
					,86	56,59,62,65,68,71,	74,77,78,80,8
56,59,62,65,68,71,							
74,77,78,80,83,86							
					1,	110,113,116,119,	122,125,128,1
110,113,116,119,							
122,125,128,131,							
134,137							
					5	114,117,120,123,	126,129,132,1
114,117,120,123,							
126,129,132,135							

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Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
R16,19,23,26,29,52,	RESISTOR,FXD,CMPSN	220K OHMS	1/8 W	5 %	81349	RCR05G224JS 55,58,61,64,67,70, 73,76,79,82,8	
R63,66,69,72,75,78, 81,84,115,118,121, 124,127,130,133,136	RESISTOR,FXD,CMPSN	15K OHMS	1/8 W	5 %	81349	RCR05G153JS	
R57,60,109,112	RESISTOR,FXD,CMPSN	8.2K OHMS	1/8 W	5 %	81349	RCR05G822JS	
R34,35,54,106	RESISTOR,FXD,CMPSN	4.7K OHMS	1/8 W	5 %	81349	RCR05G472JS	
R2,5,8,10,13	RESISTOR,FXD,CMPSN	39K OHMS	1/8 W	5 %	81349	RCR05G393JS	
R3,6,9,11,14	RESISTOR,FXD,CMPSN	3.9K OHMS	1/8 W	5 %	81349	RCR05G392JS	
R49,50,87,88	RESISTOR,FXD,CMPSN	1K OHMS	1/8 W	5 %	81349	RCR05G102JS	
R45,98	RESISTOR,FXD,FILM	1MEG OHMS	1/4 W	1 %	81349	RN65C1004F	
R37,90	RESISTOR,FXD,WW	3998 OHMS	1/8 W	1/100	14742	MPC003998-01	
R38,91	RESISTOR,FXD,WW	7996 OHMS	1/8 W	1/100	14742	MPC007996-01	
R39,92	RESISTOR,FXD,WW	15,996 OHMS	1/8 W	1/100	14742	MPC015996-01	
R40,93	RESISTOR,FXD,WW	31,996 OHMS	1/8 W	1/100	14742	MPC031996-01	
R41,94	RESISTOR,FXD,WW	64K OHMS	1/8 W	1/250	14742	MPC064000-02	
R42,95	RESISTOR,FXD,WW	128K OHMS	1/8 W	1/100	14742	MPC128000-01	
R43,96	RESISTOR,FXD,WW	256K OHMS	1/8 W	1/20 %	14742	MPC256000-05	
R44,97	RESISTOR,FXD,WW	512K OHMS	1/8 W	1 %	14742	MPC512000-99	
R36,89	RESISTOR,FXD,WW	113,174 OHMS	1/8 W	1/100	14742	MPC1131R7-01	
R15,18	RESISTOR,FXD,FILM	45.5K OHMS	1/20 W	1 %	81349	RN50C4552F	
R12,21	RESISTOR,FXD,FILM	90.9K OHMS	1/20 W	1 %	81349	RN50C9092F	
R7,22	RESISTOR,FXD,CMPSN	180K OHMS	1/8 W	5 %	81349	RCR05G184JS	
R4,25	RESISTOR,FXD,CMPSN	360K OHMS	1/8 W	5 %	81349	RCR05G364JS	
R1,28	RESISTOR,FXD,CMPSN	750K OHMS	1/8 W	5 %	81349	RCR05G754JS	
R46,99	RESISTOR,FXD,CMPSN	2MEG OHMS	1/8 W	5 %	81349	RCR05G205JS	
R47,48,100,101	RESISTOR,FXD,CMPSN	3.9MEG OHMS	1/8 W	5 %	81349	RCR05G395JS	
C2	CAP,FXD,CERAMIC	5 ρF	50 V	25 %	93958	SC-5	
C1	CAP,FXD,CERAMIC	10 ρF	50 V	25 %	93958	SC-10	
C3	CAP,FXD,CERAMIC	220 ρF	50 V	25 %	93958	SC-220	
	TRANSIPAD				13103	7717-16-DAP	
A5	CKT CD ASSY,APPROX				14742	206498-11	
U1,3,4	IC,COS/MOS,HEX				02735	CD4049AD	
U2	IC,DGTL,8-BIT				04713	MC14559BAL	
U5	IC,DGTL,8-BIT				04713	MC14549BAL	
U6	IC,COS/MOS,DUAL				02735	CD4027AD	
U7,9,12,14,16	IC,EXCLUSIVE-OR	GATE,QUAD 2	INPUT		01295	SN5486J	

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
U8	RESISTOR NETWORK	2.0K OHMS	1/8 W	2 %	73138	898-1-R2.0K	
U10	IC,QUAD 2-INP,NAND	COS/MOS			02735	CD4011AD	
U11	IC,DUAL,FLIP-FLOP	14-PIN			27014	DM5474J	
U13,15,17	IC,HEX INVERTER	14 PIN			01295	SN5404J	
R2,6,9-12	RESISTOR,FXD,CMPSN	4.7K OHMS	1/4 W	5 %	81349	RCR07G472JS	
R1,3-5,7,8	RESISTOR,FXD,CMPSN	10K OHMS	1/4 W	5 %	81349	RCR07G103JS	
C4	CAP,FXD,CERAMIC	56 ρF	200 V	10 %	81349	CK05BX560K	
C5	CAP,FXD,CERAMIC	1000 ρF	200 V	10 %	81349	CK05BX102K	
C1,2,6,7	CAP,FXD,CERAMIC	0.1 μF	100 V	10 %	81349	CK05BX104K	
C3	CAP,FXD,CERAMIC	0.01 μF	100 V	10 %	81349	CK05BX103K	
A6	CKT CD ASSY,32X	COMB			14742	209508-1	
U1,5	IC,HEX INVERTER				01295	SN7404N	
U2	IC,NAND GATE	QUAD 2-INPUT			01295	SN7400N	
U3,8,11	IC,DECODER,BINARY				18324	N8250N	
U4	IC,COUNTER,BINARY				18324	N8281N	
U6	IC,NAND GATE,QUAD-2	POS INP			01295	SN74H00N	
U7	IC,MONOSTABLE MV				28480	1820-0088	
U9,10	IC,TRIP-3 INPUT GT				28480	1820-0310	
U12,15,16,17	IC,SHIFT RGTR,4-BIT				01295	SN74178N	
U14	IC,FULL ADDERS	16-PIN			01295	SN7483N	
U13	IC,FULL ADDER,2 BIT	BINARY,14PIN			01295	SN7482N	
Q1	TRANSISTOR,UNJ,SIL	50 mA	0.36 W	TO-72	80131	2N3980	
R1	RESISTOR,FXD,CMPSN	15 OHMS	1/4 W	5 %	81349	RCR07G153JS	
R2	RESISTOR,FXD,CMPSN	100 OHMS	1/4 W	5 %	81349	RCR07G101JS	
R3	RESISTOR,FXD,CMPSN	22 OHMS	1/4 W	5 %	81349	RCR07G220JS	
R4	RESISTOR,FXD,CMPSN	10K OHMS	1/4 W	5 %	81349	RCR07G103JS	
C1,3-6	CAP,FXD,CERAMIC	0.1 μF	100 V	10 %	81349	CK05BX104K	
C2	CAP,FXD,CERAMIC	1500 ρF	100 V	10 %	81349	CK05BX152K	
	TRANSIPAD				13103	7717-16-DAP	

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
A7	CKT CD ASSY,DUAL	OUT RGTR	REGISTER		14742	212194-2	
U1,2,4,5,7,8	IC,FLIP FLOP	W/ENABLE,OCT	AL,HEXTQ UAD D		01295	SN54LS377J	
U3,6	RESISTOR NETWORK	10K OHMS	1/8 W	2 %	73138	898-1-R10K	
U9	IC,HEX INVERTER				01295	SN54LS04J	
R1-4	RESISTOR,FXD,CMPSN	10K OHMS	1/8 W	5 %	81349	RCR05G103JS	
C1	CAP,FXD,ELCTLT	10 µF	35 V	20 %	8F485	DP010	
C2	CAP,FXD,CERAMIC	0.1 µF	100 V	10 %	81349	CK05BX104K	
A8,13	CKT CD ASSY,	ADDER/COMPLIMENTER			14742	212814-1	
U1-3	SWITCH,ROCKER	5 A	30 V		81073	76SB08	
U4-8	IC,4-BIT BINARY,	FULL ADDER			01295	SN54LS283J	
U9-13	IC,EXCLUSIVE-OR	GATE,QUAD 2	INPUT		01295	SN5486J	
R1-20	RESISTOR,FXD,CMPSN	10K OHMS	1/8 W	5 %	81349	RCR05G103JS	
R21	RESISTOR,FXD,CMPSN	1K OHMS	1/8 W	5 %	81349	RCR05G102JS	
C1,4	CAP,FXD,ELCTLT	22 µF	15 V	10 %	81349	CSR13D226KL	
C2,3	CAP,FXD,CERAMIC	0.1 µF	100 V	10 %	81349	CK05BX104K	
A9,14	CKT CD ASSY,BIN	TO BCD			14742	207730-2	
U1-4,8-11	IC,4 BIT FULL ADDER				02735	CD4008AE	
R1-20	RESISTOR,FXD,CMPSN	10K OHMS	1/8 W	5 %	81349	RCR05G103JS	
A10,15	CKT CD ASSY,BIN	TO BCD			14742	207733-3	
U1-6	IC,4 BIT FULL ADDER				02735	CD4008AD	
U7	IC,HEX BUFFER/CONV	CERAMIC			14742	404010-1	
U14	IC,BINARY-BCD CONV	CONVERTER			01295	SN54185AJ	
R1,3	RESISTOR,FXD,CMPSN	10K OHMS	1/8 W	5 %	81349	RCR05G103JS	
C1,3	CAP,FXD,CERAMIC	0.1 µF	100 V	10 %	81349	CK05BX104K	

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Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
A11,12,16,17	CKT CD ASSY,DIFF	LINE DRVR			14742	212815-1	
U1-11	IC,LINE DRVR	DUAL DIFF			01295	SN55183J	
C1,3	CAP,FXD,ELCTLT	22 μF	15 V	10 %	81349	CSR13D226KL	
C2,4	CAP,FXD,CERAMIC	0.1 μF	100 V	10 %	81349	CK05BX104K	
E1	TERMINAL,PIN				86577	1D3-8B	
A18	CKT CD ASSY,1200 HZPWR SPLY	SUPPLY			14742	211190-5	
U1	IC,OPNL AMPL				27014	LH0021K	
U2,3	IC,OPNL AMPL				18324	LM101AH	
	INSULATOR,MICA				91833	4658	
CR1,2	SEMICOND DVC,DIODE	3.3 V		5 %	80131	1N746A	
CR3	SEMICOND DVC,DIODE	10 mA	75 V		80131	1N4148	
C1,2	CAP,FXD,ELCTLT	470 μF	30 V	10 %	56289	109D477X9030T2	
C3	CAP,FXD,CERAMIC	3300 ρF	100 V	10 %	81349	CK05BX332K	
C4,5,13-16	CAP,FXD,CERAMIC	33 μF	50 V	10 %	81349	CK06BX334K	
C6,7	CAP,FXD,PLASTIC	0.01 μF	50 V	10 %	84411	X463UW1029.5W2	
C8	CAP,FXD,CERAMIC	5 ρF	50 V	25 %	93958	SC-5	
C9,10	CAP,FXD,CERAMIC	150 ρF	200 V	10 %	81349	CK05BX151K	
C11,12	CAP,FXD,ELCTLT	47 μF	20 V	10 %	81349	CSR13E476KM	
R1,2	RESISTOR,FXD,WW	1.5 OHMS	3 W	5 %	81349	RW69V1R5	
R3	RESISTOR,FXD,CMPSN	75K OHMS	1/4 W	5 %	81349	RCR07G753JS	
R3	RESISTOR,FXD,CMPSN	82K OHMS	1/4 W	5 %	81349	RCR07G823JS	
R3	RESISTOR,FXD,CMPSN	91K OHMS	1/4 W	5 %	81349	RCR07G913JS	
R3	RESISTOR,FXD,CMPSN	100K OHMS	1/4 W	5 %	81349	RCR07G104JS	
R3	RESISTOR,FXD,CMPSN	110K OHMS	1/4 W	5 %	81349	RCR07G114JS	
R3	RESISTOR,FXD,CMPSN	120K OHMS	1/4 W	5 %	81349	RCR07G124JS	
R3	RESISTOR,FXD,CMPSN	130K OHMS	1/4 W	5 %	81349	RCR07G134JS	
R11	RESISTOR,FXD,CMPSN	750 OHMS	1/4 W	5 %	81349	RCR07G751JS	
R11	RESISTOR,FXD,CMPSN	820 OHMS	1/4 W	5 %	81349	RCR07G821JS	
R11	RESISTOR,FXD,CMPSN	910 OHMS	1/4 W	5 %	81349	RCR07G911JS	
R11	RESISTOR,FXD,CMPSN	1K OHMS	1/4 W	5 %	81349	RCR07G102JS	
R11	RESISTOR,FXD,CMPSN	1.1K OHMS	1/4 W	5 %	81349	RCR07G112JS	
R11	RESISTOR,FXD,CMPSN	1.2K OHMS	1/4 W	5 %	81349	RCR07G122JS	
R11	RESISTOR,FXD,CMPSN	1.3K OHMS	1/4 W	5 %	81349	RCR07G132JS	

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Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
R11	RESISTOR,FXD,CMPSN	1.5K OHMS	1/4 W	5 %	81349	RCR07G152JS	
R4,8,12	RESISTOR,FXD,CMPSN	10K OHMS	1/4 W	5 %	81349	RCR07G103JS	
R5	RESISTOR,FXD,CMPSN	200K OHMS	1/4 W	5 %	81349	RCR07G204JS	
R6	RESISTOR,FXD,CMPSN	330K OHMS	1/4 W	5 %	81349	RCR07G334JS	
R7	RESISTOR,FXD,CMPSN	5.1K OHMS	1/4 W	5 %	81349	RCR07G512JS	
R9	RESISTOR,FXD,CMPSN	51 OHMS	1/4 W	5 %	81349	RCR07G510JS	
R10	RESISTOR,FXD,CMPSN	1K OHMS	1/4 W	5 %	81349	RCR07G102JS	
T1	TRANSFORMER				14742	208670-1	
A19	EXTENDER,CKT CD	80 PIN			14742	212189-1	
	CONNECTOR,RCPT,ELEC				71785	50-80C-10	
	KEY,POLARIZING				71785	474-11-76-229	
A20	EXTENDER,CKT CD				14742	211300-1	
	CONNECTOR,RCPT,ELEC				02660	225-22521-101	
	KEY,POLARIZING				71785	474-11-76-229	
	TRANSDUCER,POSN	1.5 VA	12 V	10 %	14742	801628-2	
	CONNECTOR,RCPT,ELEC				96906	MS3112E20-16P	
	CONNECTOR,PLUG,ELEC				96906	MS3116F20-16S	
PS1	POWER SUPPLY	3/4 A	12-15 V		24230	115	
	CKT CD ASSY,MOTHER				24230	1025A	
P1	RESISTOR,VAR,CERMET	1K OHMS	3/4 W	10 %	32997	3006P-1-102	

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
P2	RESISTOR,VAR,CERMET	500 OHMS	1/2 W	10 %	73138	62PR500	
R1	RESISTOR,FXD,CMPSN	68 OHMS	1/4 W	5 %	81349	RCR07G680JS	
R2,17,19,29	RESISTOR,FXD,CMPSN	470 OHMS	1/4 W	5 %	81349	RCR07G471JS	
R3,18,26	RESISTOR,FXD,CMPSN	27 OHMS	1/4 W	5 %	81349	RCR07G270JS	
R4	RESISTOR,FXD,CMPSN	750 OHMS	1/4 W	5 %	81349	RCR07G751JS	
R5,8,11,21,25	RESISTOR,FXD,CMPSN	2.2K OHMS	1/4 W	5 %	81349	RCR07G222JS	
R6	RESISTOR,FXD,WW	1.0 OHMS	2 W	10 %	75042	BWH-1R0-10%	
R7	RESISTOR,FXD,CMPSN	620 OHMS	1/4 W	5 %	81349	RCR07G621JS	
R9	RESISTOR,FXD,FILM	511 OHMS	1/8 W	1 %	81349	RN55D5110F	
R10,27	RESISTOR,FXD,CMPSN	100 OHMS	1/4 W	5 %	81349	RCR07G101JS	
R12,22	RESISTOR,FXD,CMPSN	300 OHMS	1/4 W	5 %	81349	RCR07G301JS	
R13	RESISTOR,FXD,CMPSN	1K OHMS	1/4 W	5 %	81349	RCR07G102JS	
R14	RESISTOR,FXD,FILM	3.09K OHMS	1/8 W	1 %	81349	RN55D3091F	
R15,23	RESISTOR,FXD,FILM	6.19K OHMS	1/8 W	1 %	81349	RN55D6191F	
R16	RESISTOR,FXD,CMPSN	180 OHMS	1/4 W	5 %	81349	RCR07G181JS	
R20	RESISTOR,FXD,FILM	1.21K OHMS	1/8 W	1 %	81349	RN55D1211F	
R24	RESISTOR,FXD,FILM	2.87K OHMS	1/8 W	1 %	81349	RN55D2871F	
R28	RESISTOR,FXD,CMPSN	6.8K OHMS	1/4 W	5 %	81349	RCR07G682JS	
R30	RESISTOR,FXD,WW	1.8 OHMS	2 W	5 %	75042	BWH-1R8-5%	
R31	RESISTOR,FXD,CMPSN	1.5K OHMS	1/4 W	5 %	81349	RCR07G152JS	
Z1,2	SEMICOND DVC,DIODE	7.5 V		5 %	80131	1N755A	
A1,2	IC,VOLTAGE RGLTR				07263	UA723DC	
D1-4,6,7	SEMICOND DVC,DIODE	SIL RECT	100 V		80131	1N4002	
Q1,6	TRANSISTOR,SIL,NPN	75 W	40 V		80131	2N6103	
Q2,5	TRANSISTOR,AMPL	50 mA	60 V		80131	2N2905A	
Q3	TRANSISTOR,SIL,PNP	60 V	60 V		80131	2N2907A	
Q4	TRANSISTOR,SIL,NPN	360 mA	60 V		80131	2N2484	
Q7,8	TRANSISTOR,SIL,NPN	800 mA	40 V		80131	2N2219A	
C1,2	CAP,FXD,CERAMIC	2300 ρF	50 V	10 %	24230	0494	
C3,10	CAP,FXD,CERAMIC	470 ρF	500V	10 %	59660	831-000X5F0471K	
C4,5	CAP,FXD,CERAMIC	0.001 μF	1000 V	10 %	56289	562CX5DBA102AG102K	
C6	CAP,FXD,ELCTLT	4.7 μF	10 V	10 %	81349	CS13BC475K	
C7	CAP,FXD,CERAMIC	220 ρF	500V	10 %	59660	831-000X5F0221K	
C8,9	CAP,FXD,ELCTLT	15 μF	20 V	10 %	81349	CS13BE156K	
S1	SWITCH,THERMAL				82647	20700L3-546L176-2	
T1	TRANSFORMER,PWR				24230	8884	
	TRANSFORMER,PWR				24230	8533	
	TRANSFORMER,PWR				24230	8578	
I1	LED,RED				50579	RL-209A	

Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
PS2	POWER SUPPLY	10 A	3.5-5.5V		24230	210	
	CKT CD ASSY				24230	C-1711	
L9,10	COIL,FXD,RF CHOKE	4.7 UH		10 %	00213	RFC-S-4.7	
L8	TRANSFORMER,PWR				24230	8656	
L6,7	COIL,FXD,RF CHOKE	4.7 UH		10 %	00213	RFC-S-4.7	
C38	CAP,FXD,POLYESTER	0.22 µF	200 V	20 %	84411	X663F.2220PCT200V	
C21-25,28-30	CAP,FXD,CERAMIC	0.001 µF	1000 V	10 %	56289	562CX5DBA102AG102K	
C18	CAP,FXD,ELCTLT	33 µF	10 V	10 %	56289	150D336X9010B2	
C16,17	CAP,FXD,CERAMIC	0.68 µF	50 V	20 %	51642	300-050-RFO-684M	
C14,15	CAP,FXD,CERAMIC	0.02 µF	1000 V	20 %	56289	562CZ5UAA102AM203M	
A2	CKT CD ASSY				24230	3410	
Q1	TRANSISTOR,SIL,NPN				04713	MJE340	
Q2,3	TRANSISTOR,AMPL	50 mA	60 V		80131	2N2905A	
Q6	TRANSISTOR,SIL,PNP				24230	7049	
Q7-9	TRANSISTOR,SIL,PNP	60 V	60 V		80131	2N2907A	
Q10	TRANSISTOR,SIL,NPN	360 mA	60 V		80131	2N2484	
D2	SEMICOND DVC,DIODE	RECTIFIER	400 V		8K838	VJ447	
D5-12,14-16	SEMICOND DVC,DIODE				04713	1N4937	
D20-23	SEMICOND DVC,DIODE	200 V			80131	1N4935	
Z1	SEMICOND DVC,DIODE	18 V		5 %	80131	1N967B	
Z2	SEMICOND DVC,DIODE	6.2 V	500 MW	5 %	80131	1N753A	
Z3	SEMICOND DVC,DIODE	3.3 V		5 %	80131	1N746A	
Z4	SEMICOND DVC,DIODE	7.5 V		5 %	80131	1N755A	
Z5	SEMICOND DVC,DIODE	200 V			24444	GZ51205A	
C1	CAP,FXD,ELCTLT	230 µF	250 V	T50-10	37942	TCG231T250N2L3P	
C2	CAP,FXD,TANTALUM	100 µF	30 V	10 %	37942	TLS107K030C1C	
C3,12	CAP,FXD,CERAMIC	0.001 µF	1000 V	10 %	56289	562CX5DBA102AG102K	
C6,37	CAP,FXD,ELCTLT	39 µF	10 V	10 %	56289	150D396X9010B2	
C7	CAP,FXD,ELCTLT	1 µF	35 V	10 %	56289	150D105X9035A2	
C8	CAP,FXD,ELCTLT	15 µF	20 V	10 %	56289	150D156X9020B2	
C9	CAP,FXD,ELCTLT	4000 µF	6 V	T75-10	56289	39D408G006GP4	
C10	CAP,FXD,ELCTLT	1000 µF	6 V	10 %	56289	150D108X9006S2	
C11	CAP,FXD,CERAMIC	0.0033 µF	1000 V	10 %	56289	562CX5DAA102AL332K	
C31	CAP,FXD,ELCTLT	0.68 µF	35 V	10 %	56289	150D684X9035A2	

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Table 3-1. Component List (Continued)

CIRCUIT REFERENCE DESIGNATOR	DESCRIPTION	VALUE	RATING	TOLERANCE	FMC	PART NUMBER	NATO STOCK NO.
C32,33	CAP,FXD,CERAMIC	56 μF	125 V	10 %	05079	UWH56-125H3MI	
C34	CAP,FXD,ELCTLT	2.2 μF	100 V	10 %	56289	150D225X9100B2	
R1	RESISTOR,FXD,WW	1.5 OHMS	3.25 W	5 %	44655	4334	
R2	RESISTOR,FXD,WW	15K OHMS	3 W	5 %	91637	RS-2B-153J	
R3	RESISTOR,FXD,CMPSN	120K OHMS	1/2 W	5 %	81349	RCR20G124JS	
R4,31	RESISTOR,FXD,CMPSN	100 OHMS	1/4 W	5 %	81349	RCR07G101JS	
R5,21	RESISTOR,FXD,CMPSN	150 OHMS	1/4 W	5 %	81349	RCR07G151JS	
R6	RESISTOR,FXD,CMPSN	1.5K OHMS	1/2 W	5 %	81349	RCR20G152JS	
R7,9,11,13	RESISTOR,FXD,CMPSN	10 OHMS	1/4 W	5 %	81349	RCR07G100JS	
R8,10	RESISTOR,FXD,CMPSN	2.7 OHMS	1/2 W	5 %	81349	RCR20G2R7JS	
R12	RESISTOR,FXD,CMPSN	47 OHMS	1/4 W	5 %	81349	RCR07G470JS	
R15,32	RESISTOR,FXD,CMPSN	1K OHMS	1/4 W	5 %	81349	RCR07G102JS	
R17	RESISTOR,FXD,CMPSN	47K OHMS	1/4 W	5 %	81349	RCR07G473JS	
R18	RESISTOR,FXD,CMPSN	300 OHMS	1/4 W	5 %	81349	RCR07G301JS	
R19	RESISTOR,FXD,CMPSN	43K OHMS	1/4 W	5 %	81349	RCR07G433JS	
R20	RESISTOR,FXD,WW	33 OHMS 1.5	W	5 %	44655	4074	
R22	RESISTOR,FXD,CMPSN	33 OHMS	1/4 W	5 %	81349	RCR07G330JS	
R23	RESISTOR,FXD,CMPSN	510 OHMS	1/4 W	5 %	81349	RCR07G511JS	
R25	RESISTOR,FXD,CMPSN	8.2K OHMS	1/4 W	5 %	81349	RCR07G822JS	
R26	RESISTOR,FXD,CMPSN	2.7K OHMS	1/4 W	5 %	81349	RCR07G272JS	
R27	RESISTOR,FXD,FILM	200 OHMS	1/8 W	1 %	81349	RN55D2000F	
R28	RESISTOR,FXD,CMPSN	12K OHMS	1/4 W	5 %	81349	RCR07G123JS	
R29	RESISTOR,FXD,FILM	82.5 OHMS	1/8 W	1 %	81349	RN55D82R5F	
R30	RESISTOR,FXD,CMPSN	270 OHMS	1/4 W	5 %	81349	RCR07G271JS	
R33	RESISTOR,FXD,CMPSN	360 OHMS	1/4 W	5 %	81349	RCR07G361JS	
R34	RESISTOR,FXD,CMPSN	220 OHMS	1/4 W	5 %	81349	RCR07G221JS	
R35	THERMISTER	1K OHMS			83186	31E2	
R36	RESISTOR,FXD,CMPSN	5.6K OHMS	1/4 W	5 %	81349	RCR07G562JS	
P1	RESISTOR,VAR,NONWW	500 OHMS	3/4 W	20 %	02111	62-1-1-501	
P2	RESISTOR,VAR,NONWW	100 OHMS	3/4 W	10 %	02111	43P101T626	
P3	RESISTOR,VAR,NONWW	5K OHMS	3/4 W	20 %	02111	62-1-1-502	
T1	TRANSFORMER,PWR				24230	8652	
T2	TRANSFORMER,PWR				24230	8541	
MA1	TRANSFORMER,PWR				24230	8654	
L1,2	TRANSFORMER,PWR				24230	8650	
L3	TRANSFORMER,PWR				24230	8663	
L5	TRANSFORMER,PWR				24230	8537	
S1	SWITCH,THERMAL				82647	20700L3-546L176-2	
Q4,5	TRANSISTOR,SIL,NPN				80131	2N5838	
D18	SEMICOND DVC,DIODE				8K838	VYA100X	